VT-SBC-SMARC-IMX95

Computer-on-Module

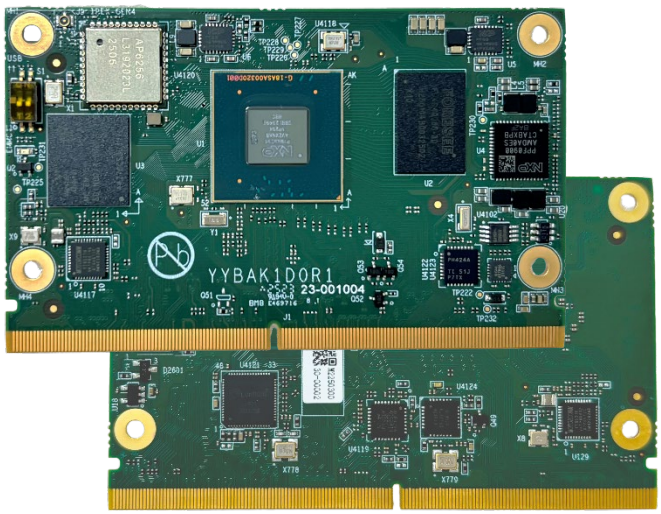
Product Brief

VT-SBC-SMARC-IMX95 Computer-on-Module (CoM) leverages the NXP iMX9594 processor to deliver robust performance in a compact SMARC 2.1 form factor. The module integrates a quad-core ARM Cortex-A55 CPU, a high-performance ARM Cortex-M7 real-time MCU, and a lower-power ARM Cortex-M33 safety MCU. It further enhances processing capabilities with a dedicated eIQ® Neutron NPU and a high-performance ARM Mali GPU, enabling efficient handling of complex computational workloads.

VT-SBC-SMARC-IMX95 delivers up to 4K@60Hz H.265/H.264 video encoding and decoding capabilities. It offers dual 4-lane or single 8-lane LVDS, delivering 1080p@60Hz resolution, and a MIPI DSI/MIPI CSI combo interface, which supports HDMI 2.0 with 4K@30Hz output via a MIPI-to-HDMI conversion IC, or native MIPI DSI with 4k@30Hz or 3840 x 1440@60Hz resolution, or MIPI CSI for camera connectivity. These features make it particularly suitable for digital signage, interactive kiosks, and medical imaging systems.

For connectivity, the module offers three Ethernet ports, including two 1 GbE ports and one 10 GbE port for high-bandwidth networking. A Wi-Fi and Bluetooth combo module is available for wireless connectivity. In addition, extensive I/O signals are available for flexible expansion. Designed for rapid deployment, the module maintains full compatibility with the i.MX 95 series processors, significantly reducing customers' time-to-market for new product development.

Exterior and Features



VT-SBC-SMARC-IMX95

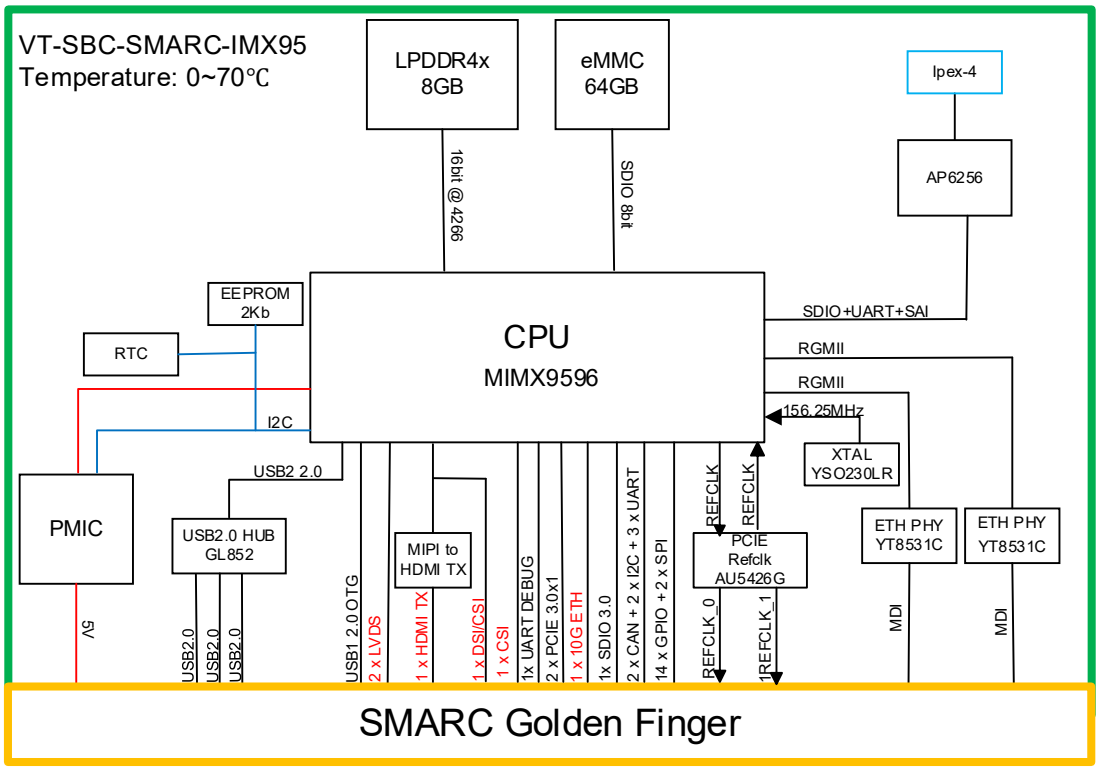
- NXP i.MX95 hexa-core CPU + two independent MCU
- 4K @60Hz H.265/H.264 video CODEC
- HDMI/MIPI DSI/LVDS for video output
- Rich I/O signals for flexible expansion
- 1/10 Gigabit Ethernet, Wi-Fi 5, Bluetooth 5.0
- Up to 2 TOPS NPU for AI acceleration
- Android and Linux Yocto systems supported
- SMARC 2.1 form factor for flexible integration

VT-SBC-SMARC-IMX95 Computer-on-Module Datasheet

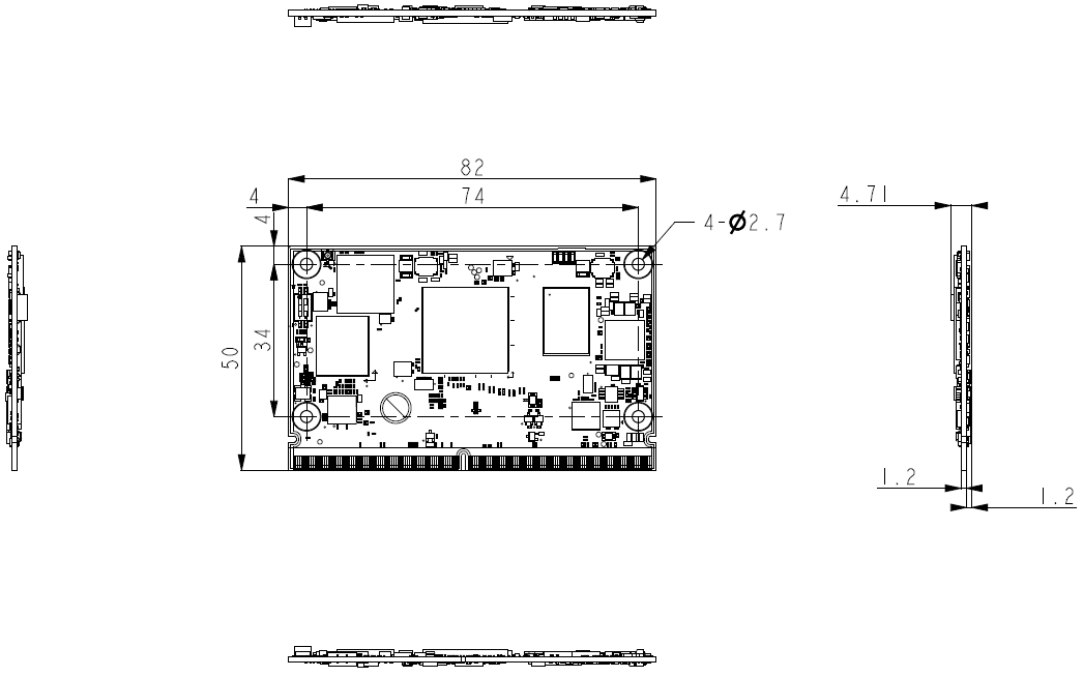
Specifications			
System	CPU	NXP i.MX9596, Hexa-core ARM Cortex-A55 processor, up to 1.8 GHz Single-core ARM Cortex-M7 real-time MCU, 800MHz Single-core ARM Cortex-M33 safety MCU, 333MHz	
	GPU	Arm Mali-G310 GPU, OpenGL ES 3.2, Vulkan 1.3, and OpenCL 3.0 supported	
	NPU	2 TOPS, support for CNN, RNN, TCN, Transformer and most neural network types	
	Memory	8GB LPDDR4x	
	Storage	64GB eMMC 5.1	
Media	Video processing	4K@60Hz H.265/H.264 video CODEC	
	Camera ISP	4K@60fps for single-channel camera / 4K@30fps for dual-channel camera	
Power	Input	5V 2.4A DC	
	Consumption	Max.: 10W (full load)	
Software	Operating system	Android, Linux Yocto, other Linux distributions (support upon request)	
	Device management	BlueSphere MDM (Optional for Android version)	
Mechanical	Dimensions	82mm x 50mm x 4.71mm (SMARC 2.1 form factor)	
Environmental Condition	Temperature	Operating: 0℃ ~ +70℃ (Optional: -40℃ ~ +85℃)	Storage: -40℃ ~ +85℃
	Humidity	5%~95% RH (Non-condensing)	

I/O		
Display (Support up to 3 displays in duplicate mode)	2 x 4-lane LVDS / 1 x 8-lane LVDS, up to 1920 x 1080 @60Hz	
	1 x HDMI 2.0, up to 4K @30Hz (default)	
	Multiplexed with: 1 x 4-lane MIPI DSI, up to 4K @30Hz or 3840 x 1440 @60Hz / 1 x 4-lane MIPI CSI	
Camera	1 x 2-Lane MIPI CSI	
	1 x 4-lane MIPI CSI (multiplexed with: HDMI / MIPI DSI)	
Audio	1 x I^2S	
Ethernet	2 x 10/100/1000Mbps (with TSN support)	1 x 10Gbps (with TSN support)
Wi-Fi and Bluetooth	Wi-Fi IEEE 802.11 a/b/g/n/ac + Bluetooth 5.0	
USB	1 x USB 2.0 OTG	4 x USB 2.0 host
UART	3 x Communication UART (1.8V)	1 x Debug UART (1.8V)
CAN	2 x CAN	
GPIO	14 x GPIO (Max.)	
SPI	2 x SPI	
I^2C	2 x I^2C	
PCIe	2 x PCIe 3.0 x1	
SDIO	1 x 4-Bit SDIO 3.0	
ADC	8 x ADC input	
Key	1 x Boot mode switch	
Watchdog Timer	Supported	
RTC	Supported	

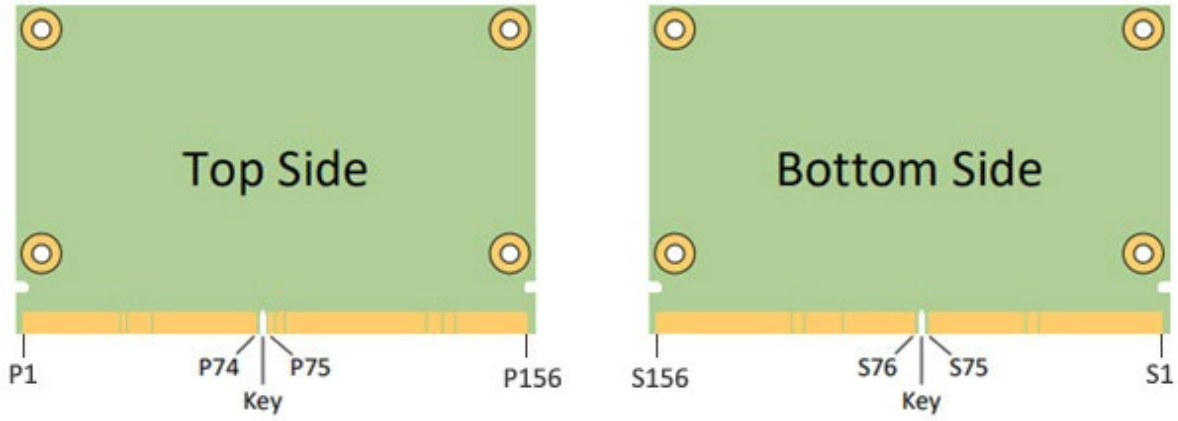
Block Diagram



Product Outlines



Edge Connector Pinout



Primary (Top) Side	Function	I/O	I/O Level	Description
P1	NC	-	-	No connection
P2	GND	P	-	Ground
P3	MIPI_CSI_1_CLK_P	Clock output	-	MIPI CSI 1 differential clock +
P4	MIPI_CSI_1_CLK_N	Clock output	-	MIPI CSI 1 differential clock -
P5	NC	-	-	No connection
P6	NC	-	-	No connection
P7	MIPI_CSI_1_RXD0_P	I	-	MIPI CSI 1 receive data 0 +
P8	MIPI_CSI_1_RXD0_N	I	-	MIPI CSI 1 receive data 0 -
P9	GND	P	-	Ground
P10	MIPI_CSI_1_RXD1_P	I	-	MIPI CSI 1 receive data 1 +
P11	MIPI_CSI_1_RXD1_N	I	-	MIPI CSI 1 receive data 1 -
P12	GND	P	-	Ground
P13	MIPI_CSI_1_RXD2_P	I	-	MIPI CSI 1 receive data 2 +
P14	MIPI_CSI_1_RXD2_N	I	-	MIPI CSI 1 receive data 2 -
P15	GND	P	-	Ground
P16	MIPI_CSI_1_RXD3_P	I	-	MIPI CSI 1 receive data 3 +
P17	MIPI_CSI_1_RXD3_N	I	-	MIPI CSI 1 receive data 3 -
P18	GND	P	-	Ground
P19	GBE_0_MDI3_N	I/0	-	GBE 0 media dependent interface 3-
P20	GBE_0_MDI3_P	I/0	-	GBE 0 media dependent interface 3+
P21	NC	-	-	No connection
P22	GBE_0_LINK1000_LED	O	3.3V (PD)	GBE 0 1000Mbps link indicator, active high

Primary (Top) Side	Function	I/O	I/O Level	Description
P23	GBE_0_MDI2_N	I/O	-	GBE 0 media dependent interface 2-
P24	GBE_0_MDI2_P	I/O	-	GBE 0 media dependent interface 2+
P25	GBE_0_ACT_LED	O	3.3V (PU)	GBE 0 activity indicator, active low
P26	GBE_0_MDI1_N	I/O	-	GBE 0 media dependent interface 1-
P27	GBE_0_MDI1_P	I/O	-	GBE 0 media dependent interface 1+
P28	GBE0_CTREF	P	-	Center tap of network transformer for GBE 0
P29	GBE_0_MDI0_N	I/O	-	GBE 0 media dependent interface 0-
P30	GBE_0_MDI0_P	I/O	-	GBE 0 media dependent interface 0+
P31	NC	-	-	No connection
P32	GND	P	-	Ground
P33	SDIO_WP	O	1.8V	SDIO write protect
P34	SDIO_CMD	O	1.8V	SDMMC 0 command/response
P35	SDIO_CD#	I	1.8V	SDMMC 0 card detection
P36	SDIO_CK	Clock output	1.8V	SDMMC 0 clock
P37	SDIO_POWER_EN	O	3.3V (PU)	SDMMC 0 power enable
P38	GND	P	-	Ground
P39	SDIO_D0	I/O	3.3V/1.8V	SDMMC 0 data 0
P40	SDIO_D1	I/O	3.3V/1.8V	SDMMC 0 data 1
P41	SDIO_D2	I/O	3.3V/1.8V	SDMMC 0 data 2
P42	SDIO_D3	I/O	3.3V/1.8V	SDMMC 0 data 3
P43	SPI_0_CS0#	O	1.8V	SPI 0 chip select
P44	SPI_0_CK	O	1.8V	SPI 0 clock
P45	SPI_0_DIN	I	1.8V	SPI 0 master in slave out
P46	SPI_0_DO	O	1.8V	SPI 0 master out slave in
P47	GND	P	-	Ground
P48	NC	-	-	No connection
P49	NC	-	-	No connection
P50	GND	P	-	Ground
P51	NC	-	-	No connection
P52	NC	-	-	No connection
P53	GND	P	-	Ground
P54	SPI_1_CS0#	O	1.8V	SPI 1 master chip select 0
P55	NC	-	-	No connection
P56	SPI_1_CK	O	1.8V	SPI 1 clock

Primary (Top) Side	Function	I/O	I/O Level	Description
P57	SPI_1_DIN	I	1.8V	SPI 1 master in slave out
P58	SPI_1_DO	O	1.8V	SPI 1 master out slave in
P59	GND	P	-	Ground
P60	OTG_USB2.0_0_DP	I/O	-	USB 2.0 port 0 OTG data +
P61	OTG_USB2.0_0_DN	I/O	-	USB 2.0 port 0 OTG data -
P62	NC	-	-	No connection
P63	USB2.0_0_VBUSDET	I	5V	USB 2.0 port 0 power detection
P64	USB2.0_0_OTGID	I	3.3V (PD)	USB 2.0 port 0 OTG identification (pull to ground to indicate device insertion, pull to 3.3V within 1KΩ to indicate host insertion)
P65	USB2.0_1_DP	I/O	-	USB 2.0 port 1 data + (host only)
P66	USB2.0_1_DN	I/O	-	USB 2.0 port 1 data - (host only)
P67	USB2.0_1_OC#	I	3.3V	USB 2.0 port 1 overcurrent indication
P68	GND	P	-	Ground
P69	USB2.0_2_DP	I/O	-	USB 2.0 port 2 data + (host only)
P70	USB2.0_2_DN	I/O	-	USB 2.0 port 2 data - (host only)
P71	USB2.0_2_OC#	I	3.3V	USB 2.0 port 2 overcurrent indication
P72	NC	-	-	No connection
P73	NC	-	-	No connection
P74	USB2.0_3_OC#	I	3.3V	USB 2.0 port 3 overcurrent indication
		KEY		
P75	PCIE3.0_A_RESET#	O	3.3V (PU)	PCIe 3.0 port A reset, active low
P76	USB2.0_4_OC#	I	3.3V	USB 2.0 port 4 overcurrent indication
P77	PCIE3.0_B_CLKREQ#	I	3.3V	PCIe 3.0 port B clock request, active low
P78	PCIE3.0_A_CLKREQ#	I	3.3V	PCIe 3.0 port A clock request, active low
P79	GND	P	-	Ground
P80	NC	-	-	No connection
P81	NC	-	-	No connection
P82	GND	P	-	Ground
P83	PCIE3.0_A_REFCKP	Clock output	-	PCIe 3.0 port A reference clock +
P84	PCIE3.0_A_REFCKN	Clock output	-	PCIe 3.0 port A reference clock -
P85	GND	P	-	Ground
P86	PCIE3.0_A_RX0P	I	-	PCIe 3.0 port A receiver +
P87	PCIE3.0_A_RX0N	I	-	PCIe 3.0 port A receiver -
P88	GND	P	-	Ground
P89	PCIE3.0_A_TX0P	I	-	PCIe 3.0 port A transmitter +
P90	PCIE3.0_A_TX0N	I	-	PCIe 3.0 port A transmitter -
P91	GND	P	-	Ground
P92	HDMI2.0_TX_D2P	O	-	HDMI transmit data 2 +
P93	HDMI2.0_TX_D2N	O	-	HDMI transmit data 2 -

Primary (Top) Side	Function	I/O	I/O Level	Description
P94	GND	P	-	Ground
P95	HDMI2.0_TX_D1P	O	-	HDMI 2.0 transmit data 1 +
P96	HDMI2.0_TX_D1N	O	-	HDMI 2.0 transmit data 1 -
P97	GND	P	-	Ground
P98	HDMI2.0_TX_D0P	O	-	HDMI 2.0 transmit data 0 +
P99	HDMI2.0_TX_D0N	O	-	HDMI 2.0 transmit data 0 -
P100	GND	P	-	Ground
P101	HDMI2.0_TX_CLKP	O	-	HDMI 2.0 transmit clock +
P102	HDMI2.0_TX_CLKN	O	-	HDMI 2.0 transmit clock -
P103	GND	P	-	Ground
P104	HDMI2.0_HPD	I	2.5~5V (PD)	HDMI 2.0 hot plug detection
P105	HDMI2.0_SCL	Clock output	1.8V (PU)	DDC clock line dedicated to HDMI
P106	HDMI2.0_SDA	I/O	1.8V (PU)	DDC data line dedicated to HDMI
P107	NC	-	-	No connection
P108	GPIO0/CAM0_PWR	I/O	1.8V	Default use: MIPI CSI camera 0 power enable, active high
P109	GPIO1/CAM1_PWR	I/O	1.8V	Default use: MIPI CSI camera 1 power enable, active high
P110	GPIO2/CAM0_RESET#	I/O	1.8V	Default use: MIPI CSI camera 0 reset, active low
P111	GPIO3/CAM1_RESET#	I/O	1.8V	Default use: MIPI CSI camera 1 reset, active low
P112	GPIO4	I/O	1.8V	GPIO
P113	GPIO5	I/O	1.8V	GPIO
P114	GPIO6	I/O	1.8V	GPIO
P115	GPIO7	I/O	1.8V	GPIO
P116	GPIO8	I/O	1.8V	GPIO
P117	GPIO9	I/O	1.8V	GPIO
P118	GPIO10	I/O	1.8V	GPIO
P119	GPIO11	I/O	1.8V	GPIO
P120	GND	P	-	Ground
P121	I2C_PM_CLK	Clock output	1.8V (PU)	I^2C clock for power management
P122	I2C_PM_SDA	I/O	1.8V (PU)	I^2C data for power management
P123	NC	-	-	No connection
P124	NC	-	-	No connection
P125	NC	-	-	No connection
P126	NC	-	-	No connection
P127	RESET_IN#	I	1.8V (PU)	Module reset, low active

Primary (Top) Side	Function	I/O	I/O Level	Description
P128	POWER_BTN#	I	1.8V (PU)	Power button (pull low for 10ms to trigger). The module is set to power up via VDD_IN supply without power button trigger by default.
P129	UART0_TX	O	1.8V	Debug UART 0 transmit data
P130	UART0_RX	I	1.8V (PU)	Debug UART 0 receive data
P131	UART0_RTS		1.8V	Debug UART 0 request to send
P132	UART0_CTS		1.8V (PU)	Debug UART 0 clear to send
P133	GND	P	-	Ground
P134	UART1_TX	O	1.8V (PD)	UART 1 transmit data
P135	UART1_RX	I	1.8V (PU)	UART 1 receive data
P136	UART2_TX	O	1.8V (PU)	UART 2 transmit data
P137	UART2_RX	I	1.8V (PU)	UART 2 receive data
P138	NC	-	-	No connection
P139	NC	-	-	No connection
P140	UART3_TX	O	1.8V	UART 3 transmit data
P141	UART3_RX	I	1.8V	UART 3 receive data
P142	GND	P	0V	Ground
P143	CAN0_TX	O	1.8V	CAN 0 transmit data
P144	CAN0_RX	I	1.8V	CAN 0 receive data
P145	CAN1_TX	O	1.8V	CAN 1 transmit data
P146	CAN1_RX	I	1.8V	CAN 1 receive data
P147	VDD_IN	P	5.0V	5V power input
P148	VDD_IN	P	5.0V	5V power input
P149	VDD_IN	P	5.0V	5V power input
P150	VDD_IN	P	5.0V	5V power input
P151	VDD_IN	P	5.0V	5V power input
P152	VDD_IN	P	5.0V	5V power input
P153	VDD_IN	P	5.0V	5V power input
P154	VDD_IN	P	5.0V	5V power input
P155	VDD_IN	P	5.0V	5V power input
P156	VDD_IN	P	5.0V	5V power input

Secondary (Bottom) Side	Function	I/O	I/O Level	Description
S1	I2C_CAM_1_CLK	Clock output	1.8V (PU)	I^2C clock for MIPI CSI 1
S2	I2C_CAM_1_SDA	I/O	1.8V (PU)	I^2C data for MIPI CSI 1
S3	GND	P	-	Ground
S4	NC	-	-	No connection
S5	I2C_CAM_0_CLK	Clock output	1.8V (PU)	I^2C clock for MIPI CSI 0
S6	CAM_MCK	Clock output	1.8V	Camera master clock for MIPI CSI 0&1
S7	I2C_CAM_0_SDA	I/O	1.8V (PU)	I^2C data for MIPI CSI 0
S8	MIPI_CSI_0_CLK_P	Clock output	-	MIPI CSI 0 differential clock +
S9	MIPI_CSI_0_CLK_N	Clock output	-	MIPI CSI 0 differential clock -
S10	GND	P	-	Ground
S11	MIPI_CSI_0_RXD0_P	I	-	MIPI CSI 0 receive data 0 +
S12	MIPI_CSI_0_RXD0_N	I	-	MIPI CSI 0 receive data 0 -
S13	GND	P	-	Ground
S14	MIPI_CSI_0_RXD1_P	I	-	MIPI CSI 0 receive data 1 +
S15	MIPI_CSI_0_RXD1_N	I	-	MIPI CSI 0 receive data 1 -
S16	GND	P	-	Ground
S17	GBE_1_MDI0_P	I/O	-	GBE 1 media dependent interface 0 +
S18	GBE_1_MDI0_N	I/O	-	GBE 1 media dependent interface 0 -
S19	NC	-	-	No connection
S20	GBE_1_MDI1_P	I/O	-	GBE 1 media dependent interface 1 +
S21	GBE_1_MDI1_N	I/O	-	GBE 1 media dependent interface 1 -
S22	GBE_1_LINK1000_LED	O	3.3V (PD)	GBE 1 1000Mbps link indicator, active high
S23	GBE_1_MDI2_P	I/O	-	GBE 1 media dependent interface 2 +
S24	GBE_1_MDI2_N	I/O	-	GBE 1 media dependent interface 2 -
S25	GND	P	-	Ground
S26	GBE_1_MDI3_P	I/O	-	GBE 1 media dependent interface 3 +
S27	GBE_1_MDI3_N	I/O	-	GBE 1 media dependent interface 3 -
S28	GBE1_CTREF	P	-	Center tap of network transformer for GBE 1
S29	NC	-	-	No connection
S30	NC	-	-	No connection
S31	GBE_1_ACT_LED	O	3.3V	GBE 1 activity indicator, active low
S32	NC	-	-	No connection
S33	NC	-	-	No connection
S34	GND	P	-	Ground
S35	USB2.0_4_DP	I/O	-	USB 2.0 port 4 data + (host only)
S36	USB2.0_4_DN	I/O	-	USB 2.0 port 4 data - (host only)

Secondary (Bottom) Side	Function	I/O	I/O Level	Description
S37	NC	-	-	No connection
S38	I2S_MCLK	Clock output	1.8V	I^2S 0 master clock
S39	I2S_0_LRCK	I/O	1.8V	I^2S 0 left/right swift clock
S40	I2S_0_SDOUT	O	1.8V	I^2S 0 serial data output
S41	I2S_0_SDIN	I	1.8V	I^2S 0 serial data input
S42	I2S_0_CK	Clock output	1.8V	I^2S 0 bit clock
S43	NC	-	-	No connection
S44	NC	-	-	No connection
S45	MDIO_CLK	Clock output	1.8V	Ethernet management data I/O clock
S46	MDIO_DAT	I/O	1.8V	Ethernet management data I/O data
S47	GND	P	-	Ground
S48	I2C_GP_CLK	Clock output	1.8V (PU)	I^2C general purpose clock
S49	I2C_GP_SDA	I/O	1.8V (PU)	I^2C general purpose data
S50	NC	-	-	No connection
S51	NC	-	-	No connection
S52	NC	-	-	No connection
S53	NC	-	-	No connection
S54	NC	-	-	No connection
S55	NC	-	-	No connection
S56	NC	-	-	No connection
S57	NC	-	-	No connection
S58	NC	-	-	No connection
S59	NC	-	-	No connection
S60	NC	-	-	No connection
S61	GND	P	-	Ground
S62	NC	-	-	No connection
S63	NC	-	-	No connection
S64	GND	P	-	Ground
S65	NC	-	-	No connection
S66	NC	-	-	No connection
S67	GND	P	-	Ground
S68	USB2.0_3_DP	I/O	-	USB 2.0 port 3 data + (host only)
S69	USB2.0_3_DN	I/O	-	USB 2.0 port 3 data - (host only)
S70	GND	P	-	Ground
S71	NC	-	-	No connection
S72	NC	-	-	No connection
S73	GND	P	-	Ground

Secondary (Bottom) Side	Function	I/O	I/O Level	Description
S74	NC	-	-	No connection
S75	NC	-	-	No connection
KEY				
S76	PCIE3.0_B_RESET#	O	3.3V (PU)	PCIe 3.0 port B reset, active low
S77	NC	-	-	No connection
S78	SERDES_1_RXP	I	1.2V	SerDes 1 receiver +, used for USXGMII
S79	SERDES_1_RXN	I	1.2V	SerDes 1 receiver -, used for USXGMII
S80	GND	P	-	Ground
S81	SERDES_1_TXP	I	1.2V	SerDes 1 transmitter +, used for USXGMII
S82	SERDES_1_TXN	I	1.2V	SerDes 1 transmitter -, used for USXGMII
S83	GND	P	-	Ground
S84	PCIE3.0_B_REFCKP	Clock output	-	PCIe 3.0 port B reference clock +
S85	PCIE3.0_B_REFCKN	Clock output	-	PCIe 3.0 port B reference clock -
S86	GND	P	-	Ground
S87	PCIE3.0_B_RX0P	I	1.8V	PCIe 3.0 port B receiver +
S88	PCIE3.0_B_RX0N	I	1.8V	PCIe 3.0 port B receiver -
S89	GND	P	-	Ground
S90	PCIE3.0_B_TX0P	I	1.8V	PCIe 3.0 port B transmitter +
S91	PCIE3.0_B_TX0N	I	1.8V	PCIe 3.0 port B transmitter -
S92	GND	P	-	Ground
S93	NC	-	-	No connection
S94	NC	-	-	No connection
S95	NC	-	-	No connection
S96	NC	-	-	No connection
S97	NC	-	-	No connection
S98	NC	-	-	No connection
S99	NC	-	-	No connection
S100	NC	-	-	No connection
S101	GND	P	-	Ground
S102	NC	-	-	No connection
S103	NC	-	-	No connection
S104	NC	-	-	No connection
S105	NC	-	-	No connection
S106	NC	-	-	No connection
S107	LCD1_BKLT_EN	O	1.8V	LCD 1 backlight enable
S108	LVDS_1_CLKP	Clock output	-	LVDS 1 clock +
S109	LVDS_1_CLKN	Clock output	-	LVDS 1 clock -

Secondary (Bottom) Side	Function	I/O	I/O Level	Description
S110	GND	P	-	Ground
S111	LVDS_1_D0P	O	-	LVDS 1 data 0 +
S112	LVDS_1_D0N	O	-	LVDS 1 data 0 -
S113	NC	-	-	No connection
S114	LVDS_1_D1P	O	-	LVDS 1 data 1 +
S115	LVDS_1_D1N	O	-	LVDS 1 data 1 -
S116	LCD1_VDD_EN	O	1.8V	LVDS VDD enable
S117	LVDS_1_D2P	O	-	LVDS 1 data 2 +
S118	LVDS_1_D2N	O	-	LVDS 1 data 2 -
S119	GND	P	-	Ground
S120	LVDS_1_D3P	O	-	LVDS 1 data 3 +
S121	LVDS_1_D3N	O	-	LVDS 1 data 3 -
S122	LCD1_BKLT_PWM	O	1.8V	LCD 1 backlight PWM control
S123	GPIO13	I/O	1.8V	GPIO
S124	GND	P	-	Ground
S125	LVDS_0_D0P	O	-	LVDS 0 data 0 +
S126	LVDS_0_D0N	O	-	LVDS 0 data 0 -
S127	LCD0_BKLT_EN	O	1.8V	Ground
S128	LVDS_0_D1P	O	-	LVDS 0 data 1 +
S129	LVDS_0_D1N	O	-	LVDS 0 data 1 -
S130	GND	P	-	Ground
S131	LVDS_0_D2P	O	-	LVDS 0 data 2 +
S132	LVDS_0_D2N	O	-	LVDS 0 data 2 -
S133	LCD0_VDD_EN	O	1.8V	LCD VDD enable
S134	LVDS_0_CLKP	Clock output	-	LVDS 0 clock +
S135	LVDS_0_CLKN	Clock output	-	LVDS 0 clock -
S136	GND	P	-	Ground
S137	LVDS_0_D3P	O	-	LVDS 0 data 3 +
S138	LVDS_0_D3N	O	-	LVDS 0 data 3 -
S139	I2C_LCD_CLK	Clock output	1.8V (PU)	I^2C clock for LCD 0&1
S140	I2C_LCD_SDA	I/O	1.8V (PU)	I^2C data for LCD 0&1
S141	LCD0_BKLT_PWM	O	1.8V	LCD 0 backlight PWM control
S142	GPIO12	I/O	1.8V	GPIO
S143	GND	P	-	Ground
S144	NC	-	-	No connection
S145	WDT_TIME_OUT#	O	1.8V	Watchdog timeout setup
S146	PCIE_WAKE#	O	3.3V	PCIe 3.0 wake up

Secondary (Bottom) Side	Function	I/O	I/O Level	Description
S147	VDD_RTC	P	3V	RTC battery power supply
S148	NC	-	-	No connection
S149	NC	-	-	No connection
S150	NC	-	-	No connection
S151	NC	-	-	No connection
S152	NC	-	-	No connection
S153	CARRIER_STBY	O	1.8V	The module shall drive this signal low when the system is in a standby power state.
S154	CARRIER_PWR_ON	O	1.8V	Carrier board circuits (apart from power management and power path circuits) should not be powered up until the module asserts the CARRIER_PWR_ON signal.
S155	RECOVERY	-	-	Recovery
S156	NC	-	-	No connection
S157	NC	-	-	No connection
S158	GND	-	-	Ground

Ordering Information

Ordering No.	Operating System	Memory	Storage	Form factor
VT-SBC-SMARC-IMX95-A	Android	8GB	64GB	SMARC 2.1
VT-SBC-SMARC-IMX95-Y	Linux Yocto	8GB	64GB	SMARC 2.1

Packing List	
VT-SBC-SMARC-IMX95 computer-on-module	1

Since its establishment in 2002 by two Silicon Valley entrepreneurs, Vantron Technology has been at the forefront of the connected IoT devices and IoT platform solutions. Today, Vantron boasts a global customer base that includes many Fortune Global 500 companies. Its product lines cover edge intelligent hardware, IoT communication devices, industrial displays and BlueSphere cloud platforms.

With over 20 years of experience in R&D of intelligent edge hardware, Vantron has provided users with diverse embedded solutions featuring ARM and X86 architectures. Its offerings range from Linux, Android to Windows, from embedded to desktop level, and from gateways to servers. In addition, it provides users with system trimming, driver transplantation and more to cater to the unique needs of its users.