Table of Contents

VT-MOB-AH-L Wi-Fi HaLow Module

1. Overview

1.1 Product Brief

VT-MOB-AH-L is a Wi-Fi HaLow module that comes in an LGA package and is powered by Morse Micro MM6108 single-chip SoC. The SoC boasts an IEEE802.11ah Wi-Fi HaLow transceiver and integrates Radio, PHY, and MAC components, allowing for operation in the sub 1GHz license exempt RF bands. Specifically designed to provide low-power, long-reach Wi-Fi connectivity for IoT applications, VT-MOB-AH-L operates between 850MHz and 950MHz bands and supports 1/2/4/8MHz channel width to provide extended transmission range and faster data rate. Moreover, the module supports SHA1 and SHA2 hash algorithms in combination with latest WPA3 protocol for enhanced connectivity security.

VT-MOB-AH-L offers an SDIO 2.0 compliant slave interface and supports SPI mode operation. Its MAC supports both station (STA) and access point (AP) roles, making it versatile for different applications.

VT-MOB-AH-L can be easily integrated to IoT communication devices to allow users to quickly build their own Wi-Fi HaLow solutions.

1.2 Features

- Packaging: LGA
- Single-stream data rate up to 32.5 Mbps @8MHz or 15 Mbps @4MHz channel bandwidth
- Support worldwide Sub-1 GHz frequency bands

  Frequency range: 850MHz~950 MHz

  Channel bandwidth options: 1/2/4/8 MHz

  Support 1 MHz and 2 MHz duplicate modes

  Max output power: 21 dBm

  Packet detection & channel equalization
- IEEE Std 802.11ah-2016 compliant
- Automatic frequency and gain control
- Support both STA and AP modes
- Security

  AES encryption engine

  SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)

  WPA3 including protected management frames (PMF)
- Host interface

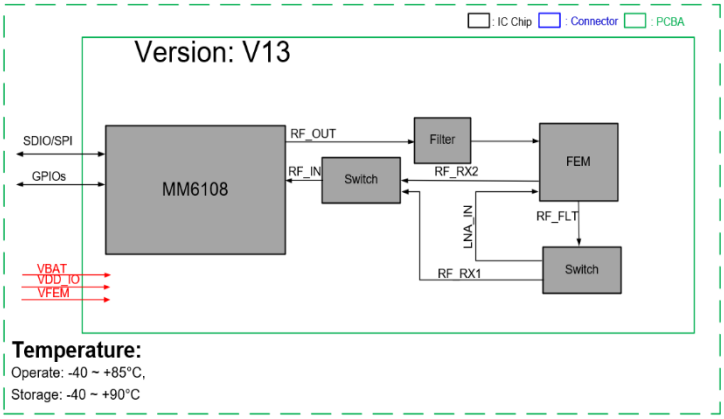
  SDIO 2.0 (slave) Default Speed (DS) at 25MHz

  SDIO 2.0 (slave) High Speed (HS) at 50MHz

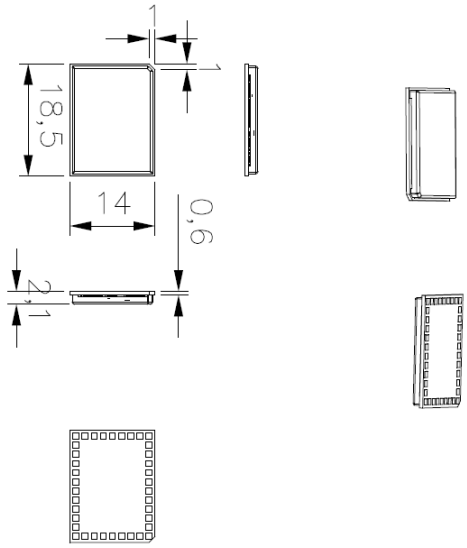
  Support both 1-bit and 4-bit data modes

  Support SPI mode operation
- BPSK & QPSK, 16-QAM & 64-QAM Modulation
- Modulation and Coding Scheme (MCS) levels: MCS 0~7 and MCS 10

1.3 Block Diagram



1.4 Product Outlines



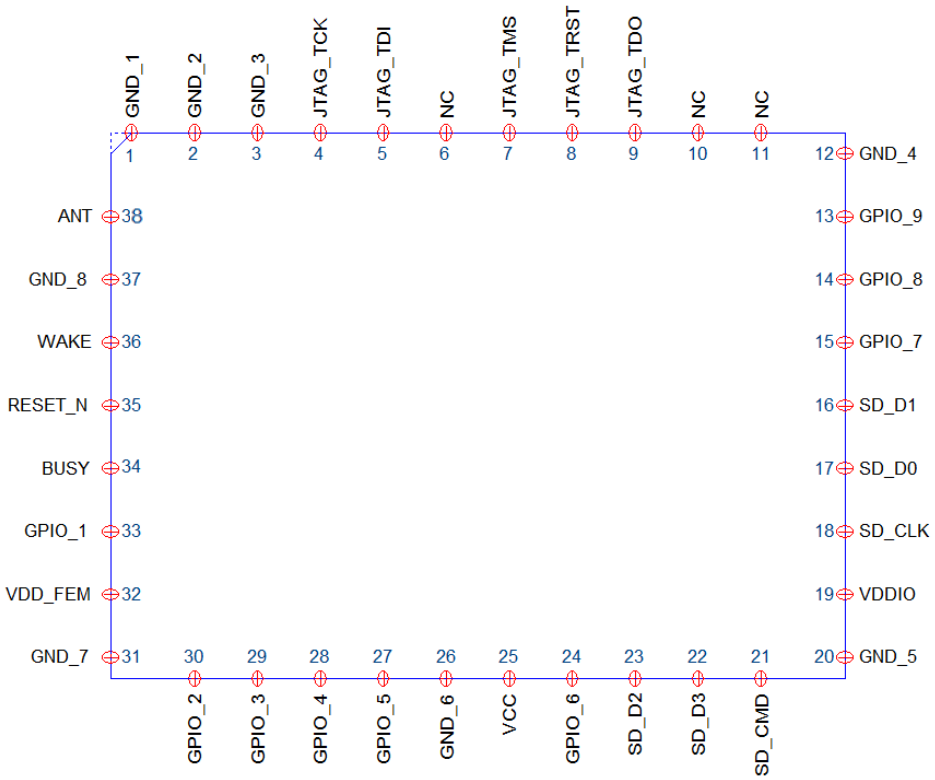
1.5 Applications

- Home automation
  - Alarm system, security cameras, smart doorbells
  - Entertainment (media streaming adapters, speakers)
  - Baby monitors
  - Garage door openers
  - Door locks
  - Smart appliances
  - Energy management
  - Voice control frontends
  - Consumer robotics
- Portables & Wearables
  - Smart watches
  - Smart glasses
  - Health trackers
- Building automation
  - Building access control & security
  - HVAC & air quality control
  - Smart city network
  - Commercial robotics
  - EV battery charger telemetry
  - Vehicle firmware OTA update
- Retail & Logistics
  - Digital signage
  - Kiosks / POS / vending machine
  - Fleet management
  - Inventory management / scanners
- Industrial Automation
  - Autonomous mobile robotics
  - Material handlers / trackers

1.6 Specifications

VT-MOB-AH-L					
Major Chipset	Morse Micro MM6108 HaLow SoC				
I/O	Host interface	1 x SDIO/SPI			
	GPIO	9 x GPIO			
	JTAG	Supported			
WLAN Features	Wi-Fi standard	IEEE 802. 11ah			
	Frequency range (Sub 1 GHz bands)	850MHz ~ 950MHz			
	Channel bandwidth	1 / 2 / 4 /8 MHz			
	Data rate	1 MHz	2 MHz	4 MHz	8 MHz
		3.33Mbps (Max.)	7.22Mbps (Max.)	15Mbps (Max.)	32.5Mbps (Max.)
	Security	AES encryption engine SHA1 and SHA2 hash algorithms (SHA-256, SHA-384, SHA-512) WPA3 including protected management frames (PMF)			
Mechanical	Dimensions	18.5mm x 14mm x 2.1mm			
	Voltage	VBAT: 3.3V	VDD_FEM: 3.3V	VDDIO: 3.3V	
	Temperature	Operating: -40℃~+85℃	Storage: -40℃~+90℃		
	Humidity	Less than 85% (Non-condensing)			
	Packaging	LGA			
	Certificate	FCC, IC, CE			

1.7 Pinout



Pin	Name	Type	Primary Function	Other Function
1	GND_1	Power	Ground	
2	GND_2	Power	Ground	
3	GND_3	Power	Ground	
4	JTAG_TCK	I	JTAG Clock	
5	JTAG_TD①	I	JTAG Data In	
6	NC	NC	Do Not Connect	
7	JTAG_TMS①	I	JTAG Mode Select	
8	JTAG_TRST	I	JTAG Reset	
9	JTAG_TDO①	O	JTAG Data Out	
10	NC	NC	Do Not Connect	
11	NC	NC	Do Not Connect	
12	GND_4	Power	Ground	
13	GPIO_9②	I/O	General Purpose IO9	
14	GPIO_8②	I/O	General Purpose IO8	
15	GPIO_7②	I/O	General Purpose IO7	UART1_TX④
16	SD_D1③	I/O	SDIO D1	SPI_INT
17	SD_D0③	I/O	SDIO D0	SPI_MISO
18	SD_CLK	I/O	SDIO Clock	SPI_SCK

Pin	Name	Type	Primary Function	Other Function
19	VDDIO	Power	3.3V VDD_IO Supply	
20	GND_5	Power	Ground	
21	SD_CMD③	I/O	SDIO Command	SPI_MOSI
22	SD_D3③	I/O	SDIO D3	SPI_CS
23	SD_D2③	I/O	SDIO D2	
24	GPIO_6②	I/O	General Purpose IO6	UART1_RX④
25	VCC	Power	3.3V VBAT Supply	
26	GND_6	Power	Ground	
27	GPIO_5②	I/O	General Purpose IO5	I2C_SCL④
28	GPIO_4②	I/O	General Purpose IO4	I2C_SDA④
29	GPIO_3②	I/O	General Purpose IO3	UART0_TX, PWM1_3④
30	GPIO_2②	I/O	General Purpose IO2	UART0_RX, PWM1_2④
31	GND_7	Power	Ground	
32	VDD_FEM	Power	3.3V Front end Module Supply	
33	GPIO_1②	I/O	General Purpose IO1	PWM1_1④
34	BUSY	O	Wi-Fi BUSY	
35	RESET_N⑤	I	System Reset	
36	WAKE⑤	I	Wake	
37	GND_8	Power	Ground	
38	ANT	Analog	Antenna	

Note:

① JTAG pins should be tied to GND via a 10k ohm pull-down resistor

② All unused GPIOs should be tied to GND via a 10k ohm pull-down resistor

③ All SDIO bus pins should be pulled up with a 10k-100k ohm resistor as per the SDIO standard

④ Pending software support

⑤ Supplied from VBAT domain. Other digital pins are driven by VDDIO domain

2. System Design

2.1 Power Management

The power for VT-MOB-AH-L is derived from a 3.0 to 3.6V supply provided on pins VBAT and VDD_FEM. VBAT powers the internal circuitry of the MM6108 and VDD_FEM powers the on-board ultra-long-range power amplifier.

VDDIO sets the IO voltage of the MM6108 and should be connected to the same power supply as the host MCU. There are no strict power-up sequencing requirements, however the voltage on VDDIO must not exceed VBAT.

2.2 Interfaces

■ Digital interfaces

All unused digital IO pins must be pulled up or down to ensure they do not float. Failure to do so will result in a higher leakage current on the VDDIO supply.

■ SDIO host requirements

VT-MOB-AH-L implements a host interface that supports SDIO 2.0 and SPI. Please refer to 2.3 Recommended Usage Schematics for the configuration of SDIO/SPI.

At a minimum, 2 x GPIOs are required as a CMOS output to drive the RESET and WAKE signals. If power save is used, a third GPIO is needed, set as a CMOS input to receive the BUSY signal from the module.

The SDIO data and command lines should be pulled up with 10k-100k ohm resistors as per the SDIO 2.0 specification.

■ SPI host requirements

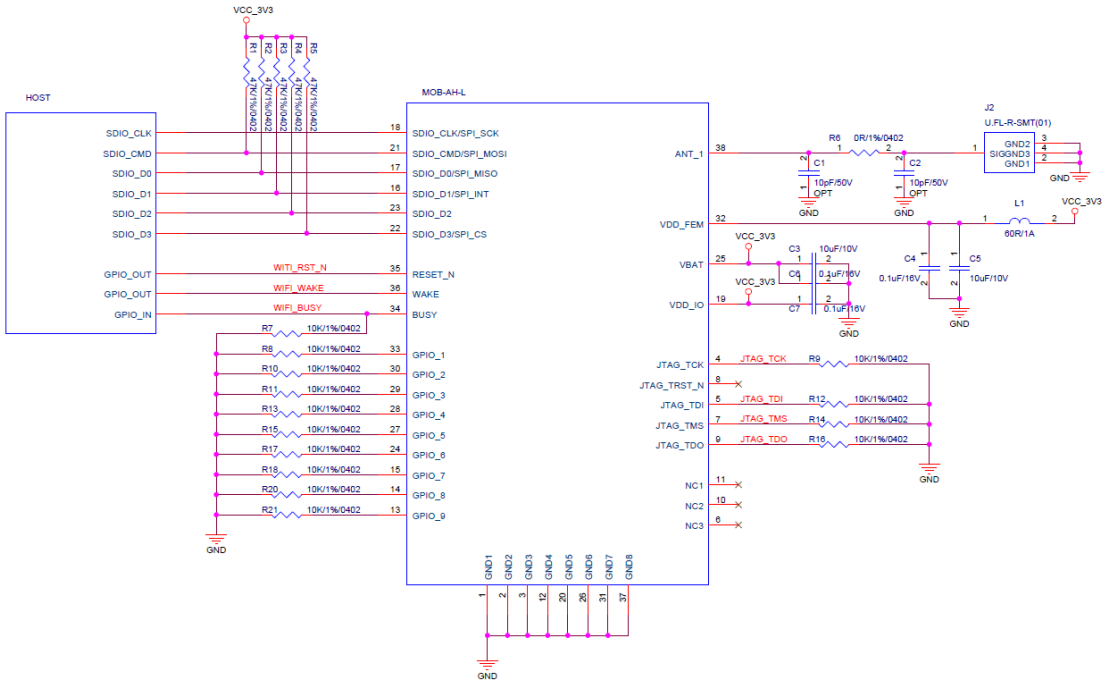
Please refer to 2.3 Recommended Usage Schematics for the configuration of SDIO/SPI.

When interfacing VT-MOB-AH-L with a CPU host via SPI, consider the following recommendations to achieve the best throughput:

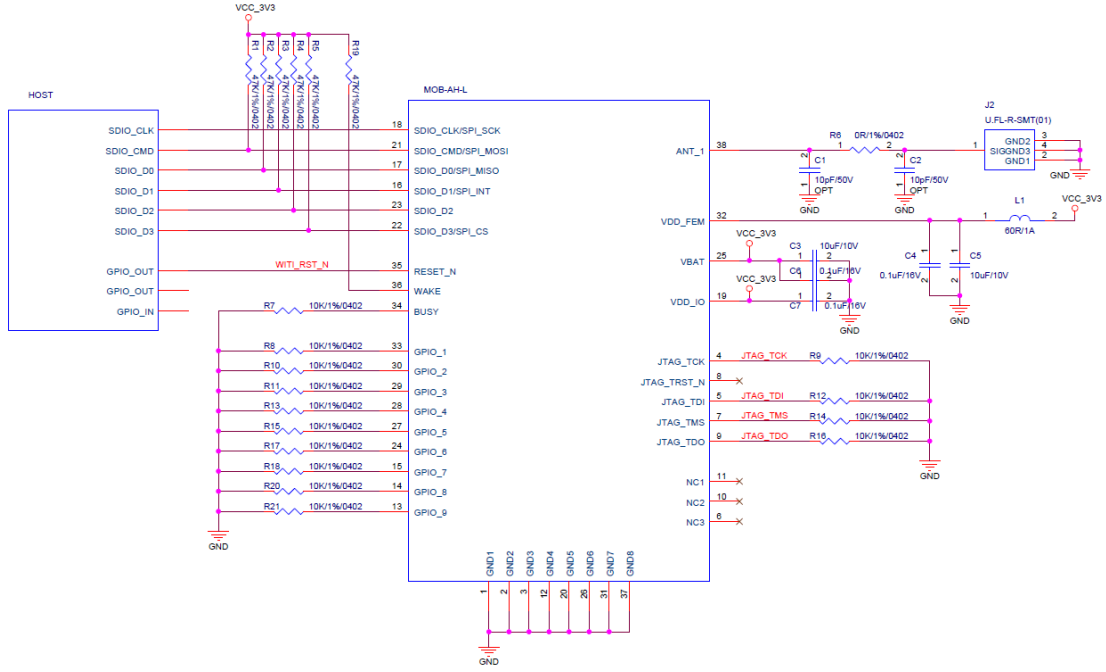
- The host should support level-triggered interrupts.
- The host should support full-duplex SPI mode.
- The host should support DMA backed transactions on the SPI bus.

Standard SPI can achieve up to 25 Mbps at 50 MHz but this will reduce significantly if there is no DMA support. For example, an SPI interface with an 8-byte buffer per transaction might only achieve 2Mbps throughput on the SPI bus.

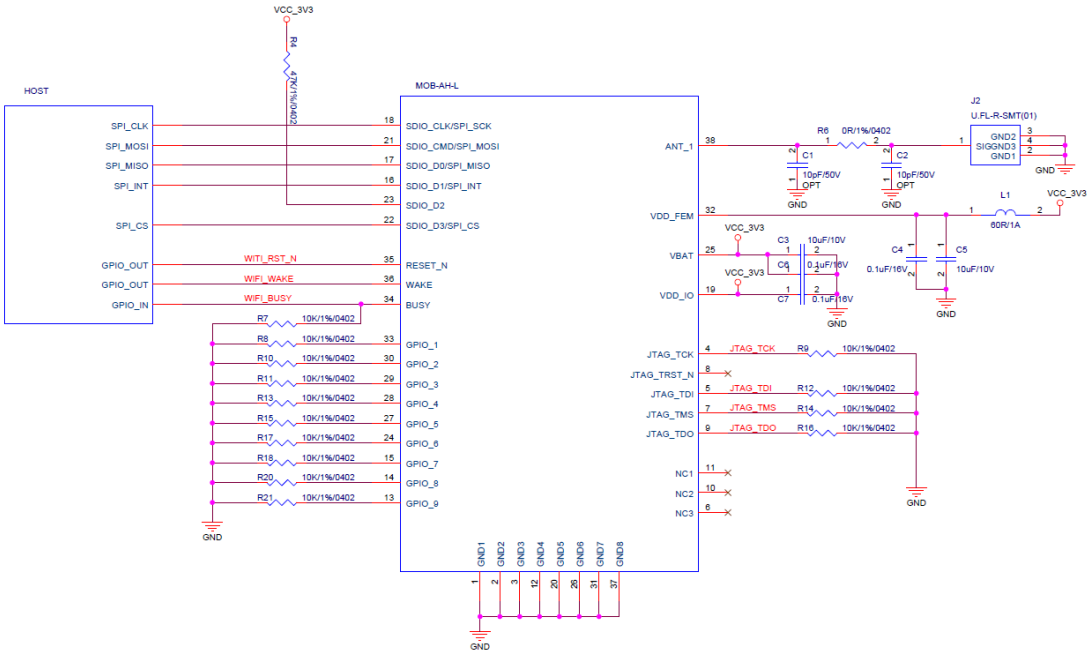
2.3 Recommended Usage Schematics



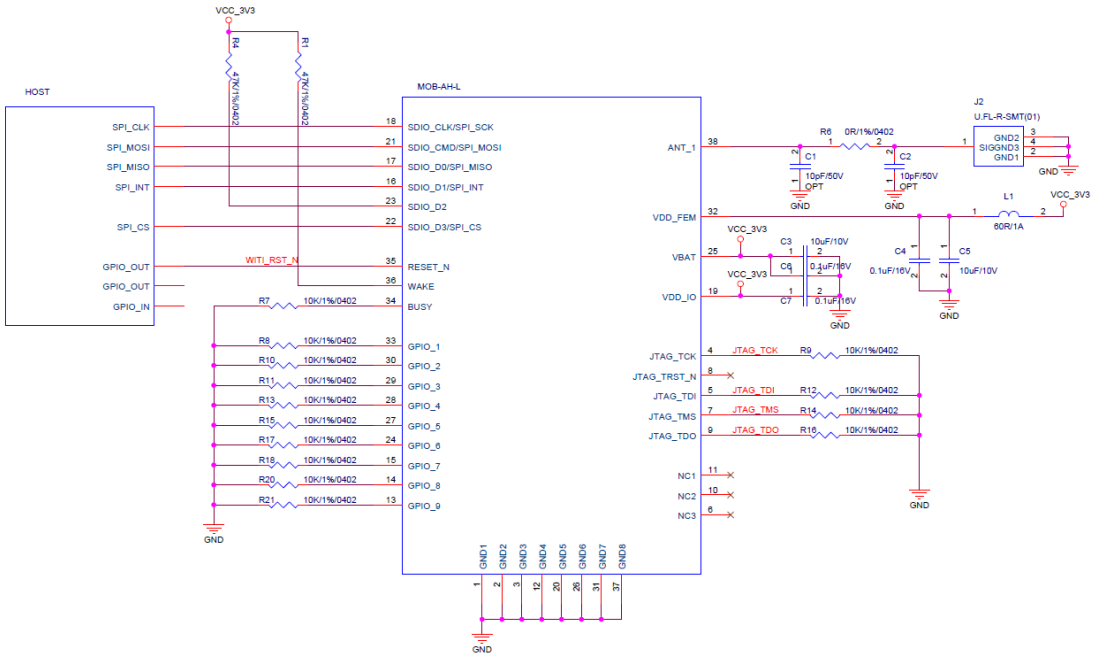
SDIO configuration



SDIO configuration with no power save



SPI configuration

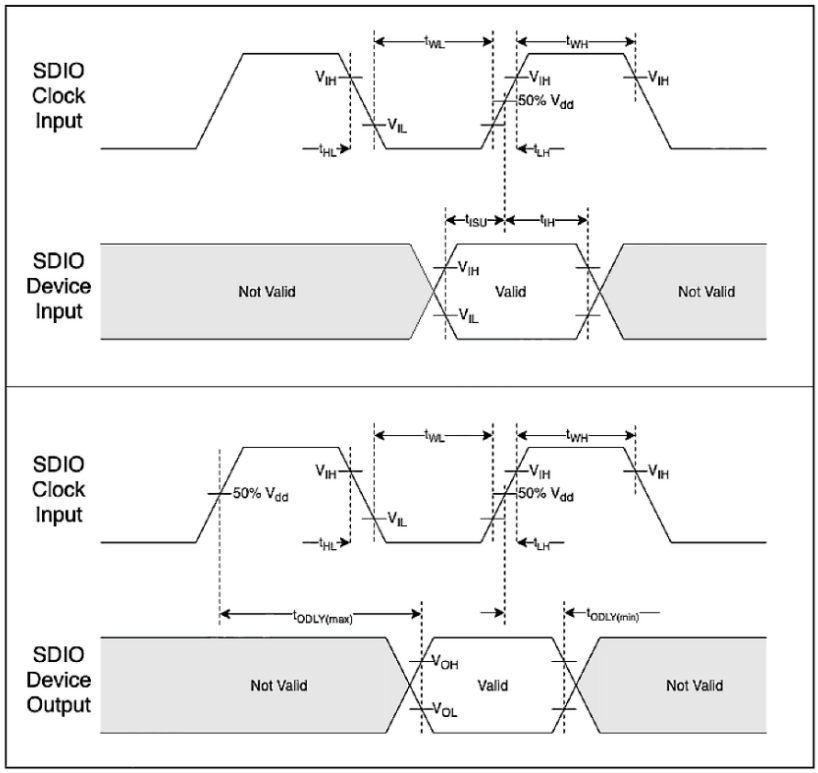


SPI configuration with no power save

2.4 Timing Sequence

■ SDIO bus timing

The SDIO interface supports a clock rate up to 50MHz.



Parameter	Min.	Max.
Clock parameters		
Clock frequency	0 MHz	50 MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

■ SPI bus timing

The SPI interface supports a clock rate up to 50MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Stress beyond absolute maximum ratings may cause permanent damage to the module. Functional operation is guaranteed for recommended operation conditions only. Operation of the device outside of recommended conditions may result in reduced lifetime and/or reliability problems even if the absolute maximum ratings are not exceeded.

Parameter	Min.	Typ.	Max.	Unit
VBAT voltage	-0.3	-	4.3	V
VDD_FEM voltage	-0.3	-	4.3	V
Voltage on digital I/O pin	-0.3	-	4.3	V
Voltage on analog/RF pin	-0.3		1.2	V
Storage temperature	-40	-	125	℃
RF input power (CW)	-	-	6	dBm

3.2 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient temperature	-40	25	85	℃
VBAT voltage	3.0	3.3	3.6	V
VDD_FEM voltage	3.0	3.3	3.6	V
VDDIO*	1.62	3.3	3.6	V
Voltage on digital I/O pin	0	3.3	VDDIO	V
RESET / WAKE I/O Voltage	0	3.3	VBAT	V

* VDDIO should not exceed VBAT.

Unless otherwise specified, performance specifications are achieved under typical operating conditions.

3.3 Power Consumption

Transmit power consumption

Mode	Condition	VBAT Current			VDD_FEM Current			Unit
	VBAT/VDDIO/ VDD_FEM =3.3V	Min.	Typ.	Max.	Min.	Typ.	Max.	
Transmit current (MCS0, 21dBm, 100% D.C.)	1 MHz channel bandwidth	54	57	73	151	152	163	mA
	2 MHz channel bandwidth	54.5	60	73	150.5	152	159.5	mA
	4 MHz channel bandwidth	60.5	66	79.5	146.5	151	156	mA
	8 MHz channel bandwidth	71	78	91.5	142.5	147	153	mA
Transmit current (MCS7, 17dBm, 100% D.C.)	1 MHz channel bandwidth	48	51	62.5	98.5	104	112	mA
	2 MHz channel bandwidth	51.5	55	66.5	97.5	104	112	mA
	4 MHz channel bandwidth	57	62	73	93.5	102	108.5	mA
	8 MHz channel bandwidth	68	72	84	91	99	105.5	mA

Receive power consumption

Mode	Condition	VBAT Current			VDD_FEM Current			Unit
	VBAT/VDDIO/ VDD_FEM =3.3V	Min.	Typ.	Max.	Min.	Typ.	Max.	
Listen	1 MHz channel bandwidth	25	26	35.5	4	4.5	4.7	mA
	2 MHz channel bandwidth	26	28	35				mA
	4 MHz channel bandwidth	30	32	40				mA
	8 MHz channel bandwidth	35	37	45.5				mA
Active receive MCS7	1 MHz channel bandwidth	26.5	26	35.5				mA
	2 MHz channel bandwidth	30	30	39.5				mA
	4 MHz channel bandwidth	37.5	40	49				mA
	8 MHz channel bandwidth	54	53	67				mA
Active receive MCS0	1 MHz channel bandwidth	28	26	37				mA
	2 MHz channel bandwidth	29.5	28	38.5				mA
	4 MHz channel bandwidth	36	36	47				mA
	8 MHz channel bandwidth	50	48	62.5				mA

Sleep power consumption

Mode	Condition	VBAT Current			VDD_FEM Current			Unit
	VBAT/VDDIO/ VDD_FEM =3.3V	Min.	Typ.	Max.	Min.	Typ.	Max.	
Deep sleep	RC Oscillator on, wake up timer configurable	0.8	1	1.8	0.001	0.05	0.55	μA

DTIM3 power consumption

Mode	Condition	VBAT Current			VDD_FEM Current			Unit
	VBAT/VDDIO/ VDD_FEM =3.3V 102.4ms beacon interval	Min.	Typ.	Max.	Min.	Typ.	Max.	
S1G beacons	1 MHz channel bandwidth	380	395	420	45	47	55	μA
	2 MHz channel bandwidth	380	395	420	45	47	55	μA
	4 MHz channel bandwidth	260	280	320	24	25	30	μA
	8 MHz channel bandwidth	260	280	320	24	25	30	μA
S1G beacons with proprietary DTIM signaling	1 MHz channel bandwidth	170	190	250	12	13	43	μA
	2 MHz channel bandwidth	170	190	250	12	13	43	μA
	4 MHz channel bandwidth	155	190	200	8	9	20	μA
	8 MHz channel bandwidth	155	190	200	8	9	20	μA

3.4 RF Specifications

Receiver

Sensitivities for 10% packet error rate, 1000-byte packets:

MCS index	Modulation scheme	Coding rate	Channel Bandwidth				Minimum receive sensitivity (dBm) per bandwidth			
			1 MHz	2 MHz	4 MHz	8 MHz	1 MHz	2 MHz	4 MHz	8 MHz
0	BPSK	1/2	333	722	1500	3250	-105	-103	-101	-97
1	QPSK	1/2	667	1444	3000	6500	-102	-100	-97	-93
2	QPSK	3/4	1000	2167	4500	9750	-99	-97	-95	-91
3	16-QAM	1/2	1333	2889	6000	13000	-96	-94	-91	-88
4	16-QAM	3/4	2000	4333	9000	19500	-93	-90	-88	-85
5	64-QAM	2/3	2667	5778	12000	26000	-89	-87	-84	-80
6	64-QAM	3/4	3000	6500	13500	29250	-88	-85	-83	-79
7	64-QAM	5/6	3333	7222	15000	32500	-87	-84	-81	-77
10	BPSK	1/2 x 2	167	N/A			-107	N/A		

Transmitter

Although the following transmit power levels are IEEE 802.11ah compliant, they do not take into account any backoffs needed to adhere to regional spectrum compliance (e.g., FCC, IC, TELEC).

Tx output power (1/2 MHz)	Min.	Typ.	Max.	Unit
MCS 0	20	21	22	dBm
MCS 7	16	17	18	dBm

Tx output power (4 MHz)	Min.	Typ.	Max.	Unit
MCS 0	20.5	21	22	dBm
MCS 7	16	17	18	dBm

Tx output power (8 MHz)	Min.	Typ.	Max.	Unit
MCS 0	20.5	21	21.5	dBm
MCS 7	15.5	17	17.5	dBm

4. Ordering Information

Ordering No.	SoC	Main I/Os	Operating Temp.	Mode
VT-MOB-AH-L	Morse Micro MM6108	GPIO, SDIO/SPI, JTAG	-40℃ ~ +85℃	AP, STA
* Use case: Use with Vantron G335 edge computing gateway via the SPI interface				

Packing list	
VT-MOB-AH-L Wi-Fi HaLow module	1

Optional accessories
N/A

5. Company Profile

Since its establishment in 2002 by two Silicon Valley entrepreneurs, Vantron Technology has been at the forefront of the connected IoT devices and IoT platform solutions. Today, Vantron boasts a global customer base that includes several Fortune 500 companies. Its product lines cover edge intelligent hardware, IoT communication devices, industrial displays and BlueSphere cloud device management platforms.

With over 20 years of experience in R&D of embedded edge intelligent hardware, Vantron has provided users with diverse embedded solutions featuring ARM and X86 architectures. Its offerings range from Linux to Windows, from embedded to desktop level, and from gateway to server. In addition, it provides users with system clipping, driver transplantation and other related services.