Table of Contents

VT-MOB-AH-8108 Wi-Fi HaLow Module

1. Overview

1.1 Product Brief

VT-MOB-AH-8108 is an LGA packaged Wi-Fi HaLow module based on Morse Micro's MM8108 single-chip SoC, which includes radio, PHY, and MAC sections designed to comply with IEEE 802.11ah standard. The standard provides support for operation in the sub 1GHz license exempt RF bands, providing ultra-long-range and low-power wireless connectivity.

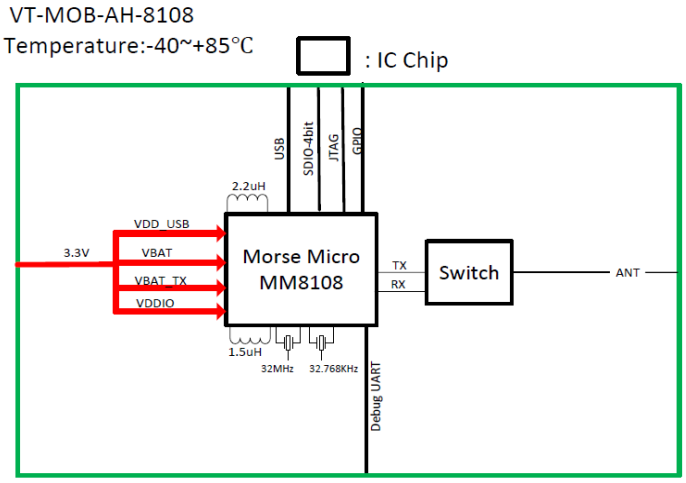
VT-MOB-AH-8108 supports single-stream data rates of up to 43.3 Mbps at the 8MHz bandwidth. It provides USB 2.0, SDIO 2.0/SPI host interfaces, and its MAC supports both station (STA) and access point (AP) role. The module is built with robust security features, including WPA3 encryption, and delivers optimal performance, thanks to its integrated power amplifier (PA), low-noise amplifier (LNA), and transmit/receive (T/R) switch.

VT-MOB-AH-8108 can be easily integrated to IoT communication devices to allow users to quickly build their own Wi-Fi HaLow solutions, such as industrial IoT, smart agriculture, and large-scale sensor networks.

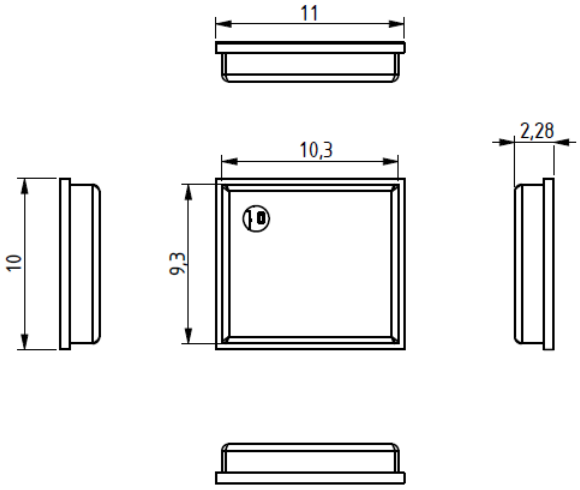
1.2 Features

- Single-stream data rate up to 43.3Mbps at 8MHz channel bandwidth
- Support worldwide Sub-1GHz frequency bands
  - Frequency range: 850MHz~950MHz
  - Channel bandwidth options: 1/2/4/8MHz
  - Max. output power: 23dBm (200mW) at 40% PA efficiency and 30% whole SoC efficiency
  - Ultra-low power receiver with integrated LNA, NF < 4dB
  - Compatible with external LNA, PA for higher power or sensitivity requirements
- 802.11ah MAC capable of WFA Wi-Fi HaLow certification
  - Support both STA and AP roles
  - Listen-Before-Talk (LBT) access with energy detect
  - 802.11 power saving
  - 802.11 fragmentation and defragmentation
  - Power-Saving Target Wake Time (TWT) support for long battery life
  - Automatic and manual MCS rate selection
- Software stack with host offload for Wi-Fi connection management
- Power Management Unit (PMU) supporting various modes of operation
- Wide spectrum of security features
  - Wi-Fi layer security including WPA3, protected management frames (PMF) and Opportunistic Wireless Encryption (OWE)
  - Hardware support for AES and SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- SDIO 2.0 compliant slave interface
  - SDIO 2.0 High-Speed at 50MHz max for 200Mbps
  - Support 1-bit and 4-bit data modes
  - Support SPI mode operation at up to 80MHz for 80Mbps
- USB 2.0 High-Speed device interface supporting up to 480Mbps
- 802.11ah OFDM PHY supporting WFA Wi-Fi HaLow certification
  - BPSK, QPSK, 16-QAM, 64-QAM & 256-QAM modulation
  - Automatic frequency & gain control
  - Packet detection & channel equalization
  - Forward Error Correction (FEC) coding & decoding
  - Support Modulation and Coding Scheme (MCS) levels 0-10
  - Support 1 MHz duplicate mode
  - Support optional traveling pilot

1.3 Block Diagram



1.4 Product Outlines



1.5 Applications

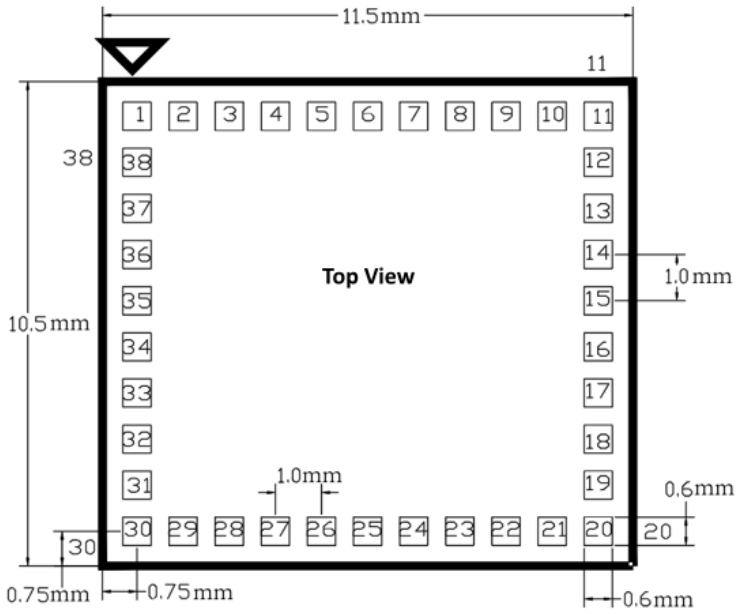
- Home Automation
  - Surveillance cameras, smart doorbells
  - Entertainment (media streaming adapters, speakers)
  - Baby monitors
  - Garage door openers
  - Door locks
  - Smart appliances
  - Energy management
  - Voice control frontends
  - Consumer robotics
- Portables & Wearables
  - Smart watches
  - Smart glasses
  - Health trackers
  - Low-power sensor networks
- Smart Building
  - Building access control & security
  - HVAC & air quality control
  - Smart city networks
  - Commercial robotics
  - EV battery charger
  - Vehicle firmware OTA update
- Retail & Logistics
  - Digital signage
  - Kiosks / POS / vending machine
  - Fleet management
  - Inventory management / scanners
- Industrial Automation
  - Autonomous mobile robotics
  - Material handlers / trackers

1.6 Specifications

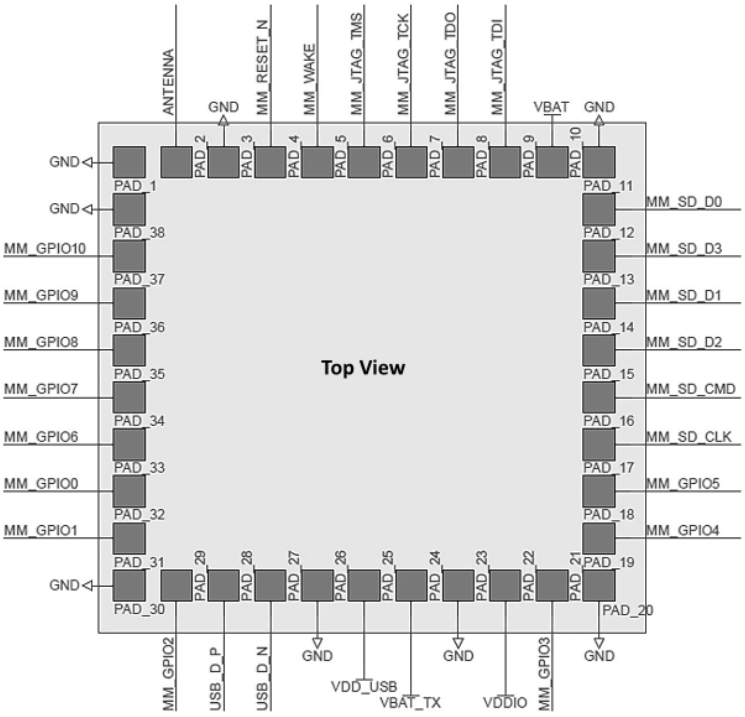
VT-MOB-AH-8108					
Major Chipset	Morse Micro MM8108 HaLow SoC				
I/O	Host interface	1 x USB 2.0 (Device)			
		1 x 1-bit/4-bit SDIO (combo with SPI)			
	GPIO	13 x GPIO			
	JTAG	Supported			
WLAN Features	Wi-Fi standard	IEEE 802. 11ah			
	Frequency range (Sub 1 GHz bands)	850MHz ~ 950MHz			
	Channel bandwidth	1 / 2 / 4 /8MHz			
	Data rate* (256-QAM)	1MHz	2MHz	4MHz	8MHz
		4.44Mbps (Max.)	8.67Mbps (Max.)	20Mbps (Max.)	43.3Mbps (Max.)
	Security	AES encryption engine			
		SHA1 and SHA2 hash algorithms (SHA-256, SHA-384, SHA-512)			
		WPA3			
		Protected management frames (PMF)			
		Opportunistic Wireless Encryption (OWE)			
Mechanical	Dimensions	11mm x 10mm x 2.28mm			
	Power	3.3V/1A DC input			
	Temperature	Operating: -40℃~+85℃		Storage: -40℃~+85℃	
	Humidity	Less than 85% (Non-condensing)			
	Packaging	LGA			
Compliance	Certification	CE, FCC, UL			

* These represent theoretical maximum values for the 256-QAM modulation scheme.

1.7 Recommended PCB Footprint



1.8 Pinout



Pin	Name	Type	Primary function	Alternate function
1	GND	Power	Ground	
2	Antenna	Analog	Antenna	
3	GND	Ground	Ground	
4	MM_RESET_N[2]	Digital I/O	Asynchronous chip reset (active low)	
5	MM_WAKE[2]	Digital I/O	External input wake from Deep Sleep and Snooze modes	
6	MM_JTAG_TMS	Digital I/O	JTAG test mode select	
7	MM_JTAG_TCK	Digital I/O	JTAG test clock	
8	MM_JTAG_TDO	Digital I/O	JTAG test data out	
9	MM_JTAG_TDI	Digital I/O	JTAG test data input	
10	VBAT	Power	3.3V VBAT supply	
11	GND	Ground	Ground	
12	MM_SD_D0[1]	Digital I/O	SDIO data 0	SPI_MISO
13	MM_SD_D3[1]	Digital I/O	SDIO data 3	SPI_CS (active low)
14	MM_SD_D1[1]	Digital I/O	SDIO data 1	SPI_INT
15	MM_SD_D2[1]	Digital I/O	SDIO data 2	
16	MM_SD_CMD[1]	Digital I/O	SDIO command	SPI_MOSI
17	MM_SD_CLK	Digital I/O	SDIO clock	SPI_SCK
18	MM_GPIO5[3]	Digital I/O	GPIO5	
19	MM_GPIO4[3]	Digital I/O	GPIO4	
20	GND	Ground	Ground	
21	MM_GPIO3[3]	Digital I/O	GPIO3	
22	VDDIO	Power	3.3V VDD supply for digital I/O	
23	GND	Ground	Ground	
24	VBAT_TX	Power	3.3V VBAT supply	
25	VDD_USB	Power	3.3V analog supply voltage for USB 2.0	
26	GND	Ground	Ground	
27	USB_D_M	Digital I/O	USB differential data line -	
28	USB_D_P	Digital I/O	USB differential data line +	
29	BUSY	Digital I/O	BUSY signal output	
30	GND	Ground	Ground	
31	MM_GPIO1[3]	Digital I/O	GPIO1	
32	MM_GPIO0[3]	Digital I/O	GPIO0	
33	MM_GPIO6[3]	Digital I/O	GPIO6	
34	MM_GPIO7[3]	Digital I/O	GPIO7	
35	MM_GPIO8[3]	Digital I/O	GPIO8	
36	MM_GPIO9[3]	Digital I/O	GPIO9	
37	MM_GPIO10[3]	Digital I/O	GPIO10	
38	GND	Ground	Ground	

Note:

1. All SDIO bus pins except SDIO_CLK should be pulled up with a 10 kΩ to 100 kΩ resistor as per the SDIO standard.
2. Supplied from VBAT domain. The VDDIO domain drives other digital pins.
3. GPIOs 0 to 10 may provide alternative functions, including SPI master, I^2C master, PWM, and UART. Contact Vantron for function customization.

2. System Design

2.1 Power Management

The VT-MOB-AH-8108 is powered from a 3.0 V to 3.6 V supply. VDDIO defines the I/O voltage level of the module, with an input range of 2.25 V to 3.6 V. It should be connected to the same power supply as the host MCU.

No strict power-up sequencing is required.

2.2 Host Interfaces

The VT-MOB-AH-8108 provides USB 2.0 and SDIO/SPI host interfaces operating at 3.3V. Please refer to Section 2.3 Recommended Usage Schematics for interface configurations.

■ USB

Pin	Name	USB 2.0 Interface
28	USB_D_P	High speed differential pin, DP
27	USB_D_M	High speed differential pin, DM
25	VDD_USB	3.3V analog supply voltage for USB 2.0

■ SDIO

When selecting a host to interface with the VT-MOB-AH-8108 via the SDIO interface, ensure the host supports SDIO 2.0 with SDIO clock speeds of up to 50 MHz. Slower clock speeds will impact the maximum achievable throughput.

The SDIO data and command lines should be pulled up with 10 kΩ to 100 kΩ resistors per the SDIO 2.0 specification.

For proper operation and to take advantage of the module's power-saving features, connect **RESET_N (pin 4)** and **WAKE (pin 5)** to standard digital outputs (CMOS logic levels). The **BUSY signal (pin 29)** should be connected to a digital input (also CMOS logic levels). Do not use open-collector or open-drain circuits, as they will cause incorrect behavior.

In applications where the module must always be on, and the power-saving features cannot be used, such as access points, the WAKE pin can be left not connected, reducing the need for GPIOs on the host processor to only one.

SPI Device

When selecting a host to interface with the VT-MOB-AH-8108 via the SPI interface, consider the following recommendations to achieve the best throughput:

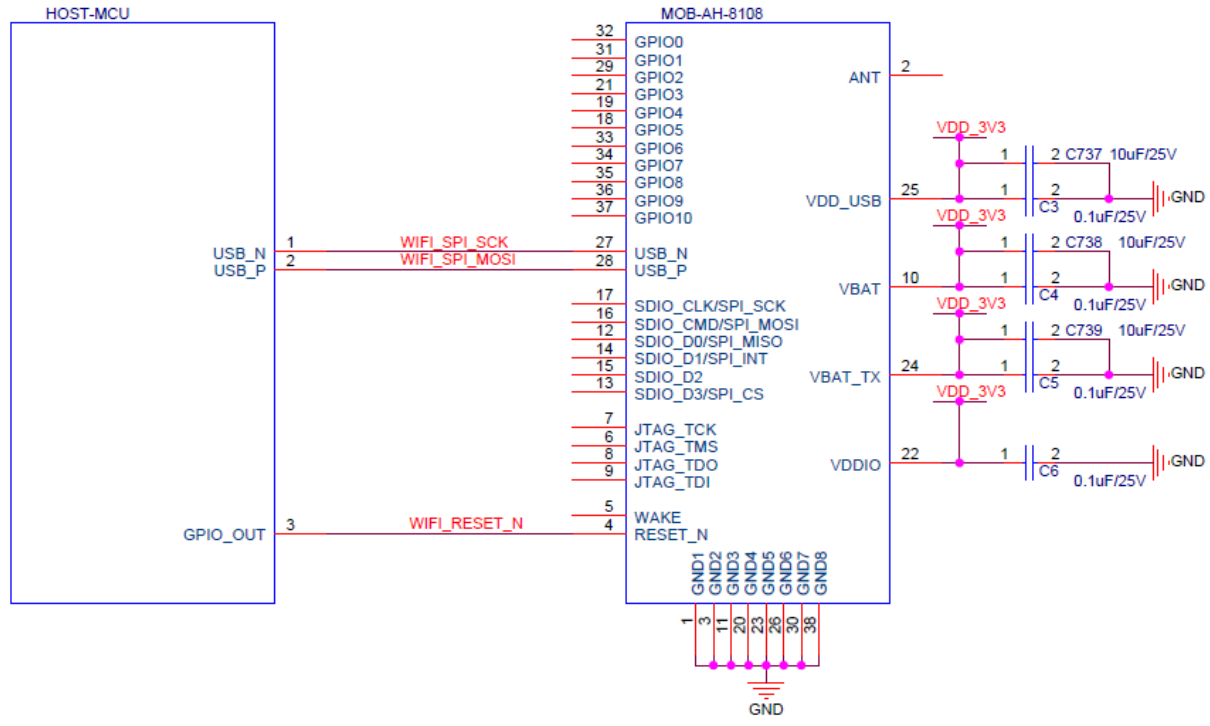
- The host must support level-triggered interrupts.
- The host must support full-duplex SPI mode.
- The host must support DMA-backed transactions on the SPI bus.

Standard SPI can achieve up to 25 Mbps at 50 MHz, which will be significantly reduced without DMA support. For example, an SPI interface with an 8-byte buffer per transaction might only achieve 2 Mbps throughput on the SPI bus.

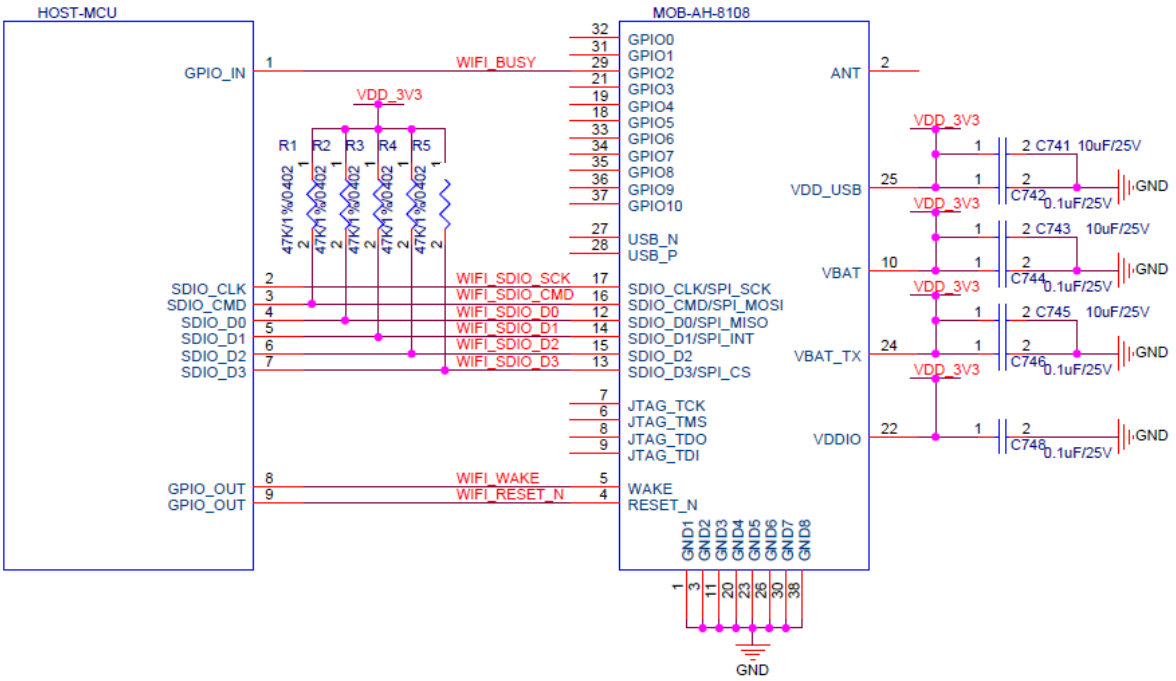
For proper operation and to take advantage of the module's power-saving features, connect **RESET (pin 4)** and **WAKE (pin 5)** to standard digital outputs (CMOS logic levels). The **BUSY signal (pin 29)** should be connected to a digital input (also CMOS logic levels). Do not use open-collector or open-drain circuits, as they will cause incorrect behavior.

In applications where the module must always be on, and the power-saving features cannot be used, such as access points, the WAKE pin can be left not connected, reducing the need for GPIOs on the host processor to only one.

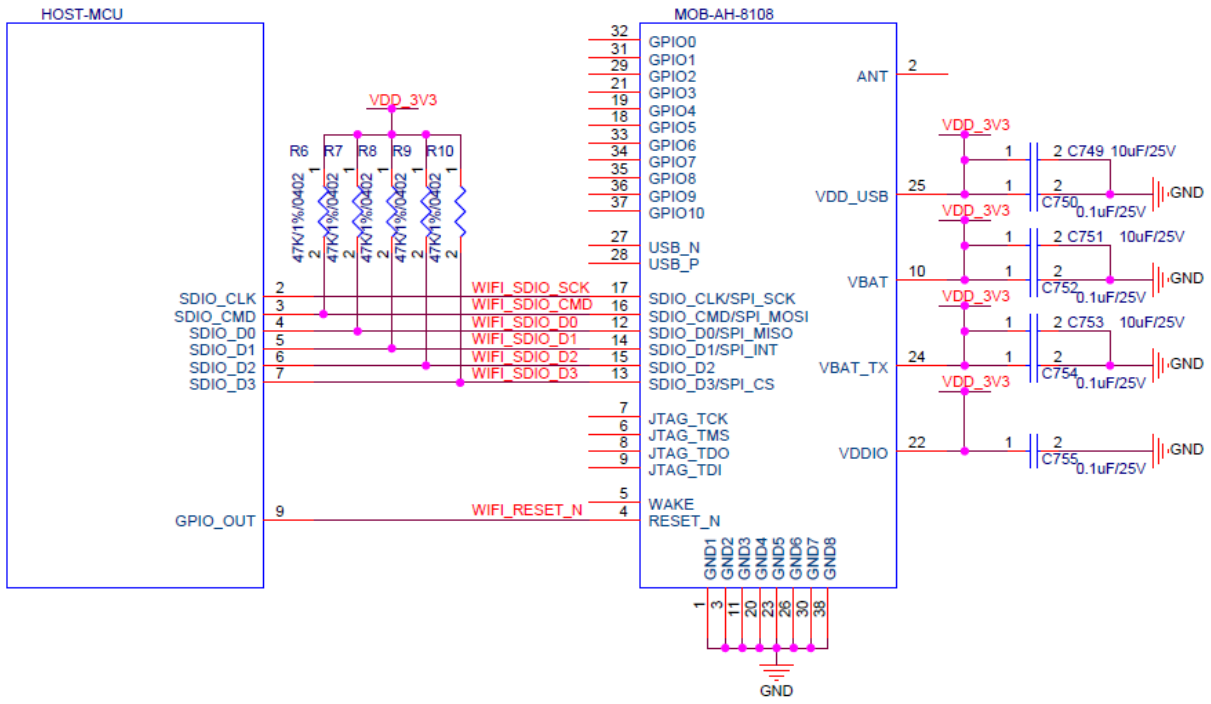
2.3 Recommended Usage Schematics



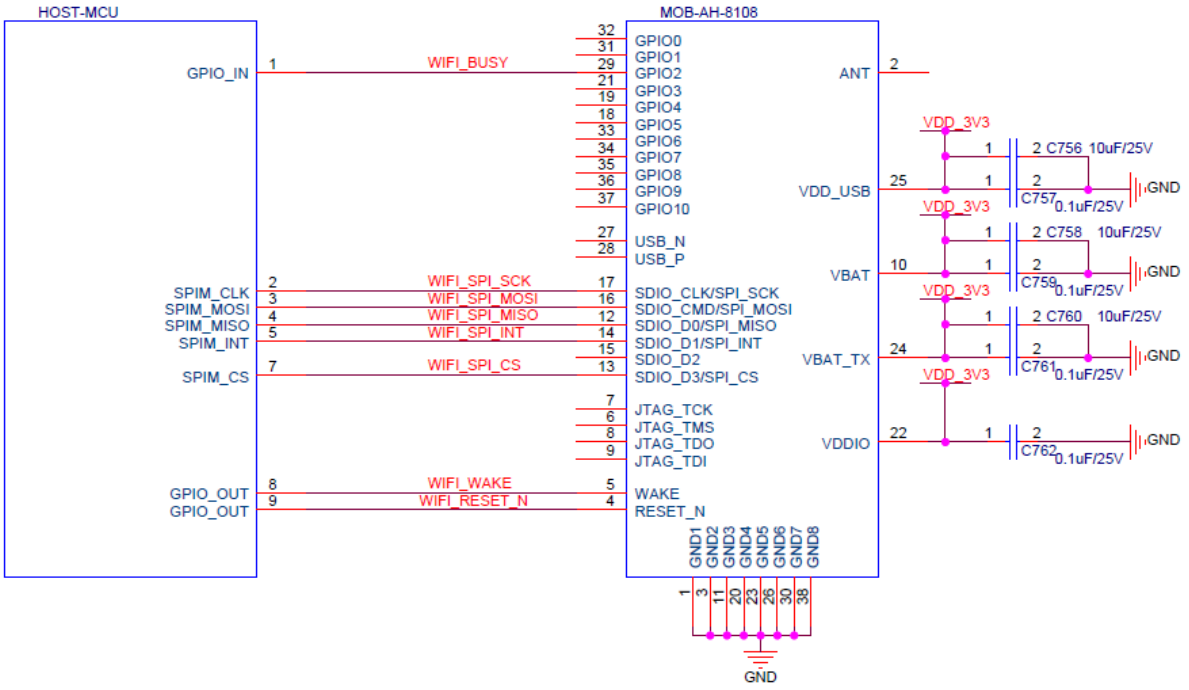
Recommended USB host interface circuit



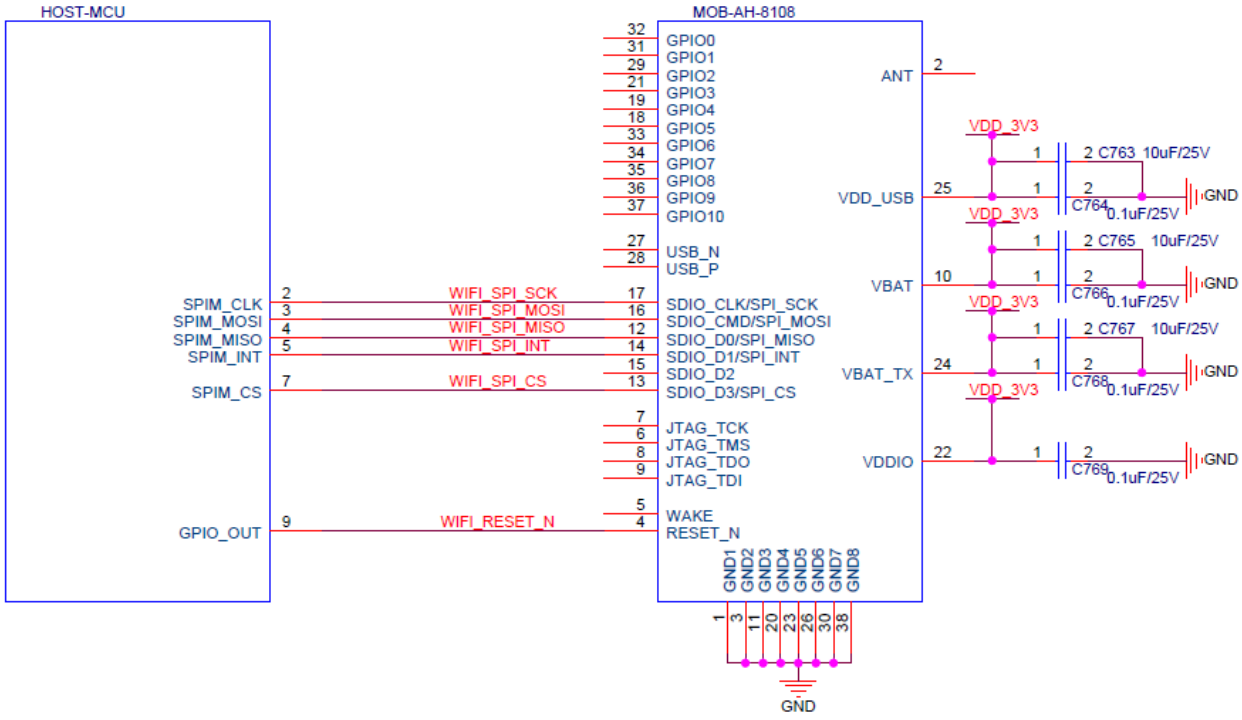
Recommended SDIO host interface circuit using power-saving features



Recommended SDIO host interface circuit for always-on applications



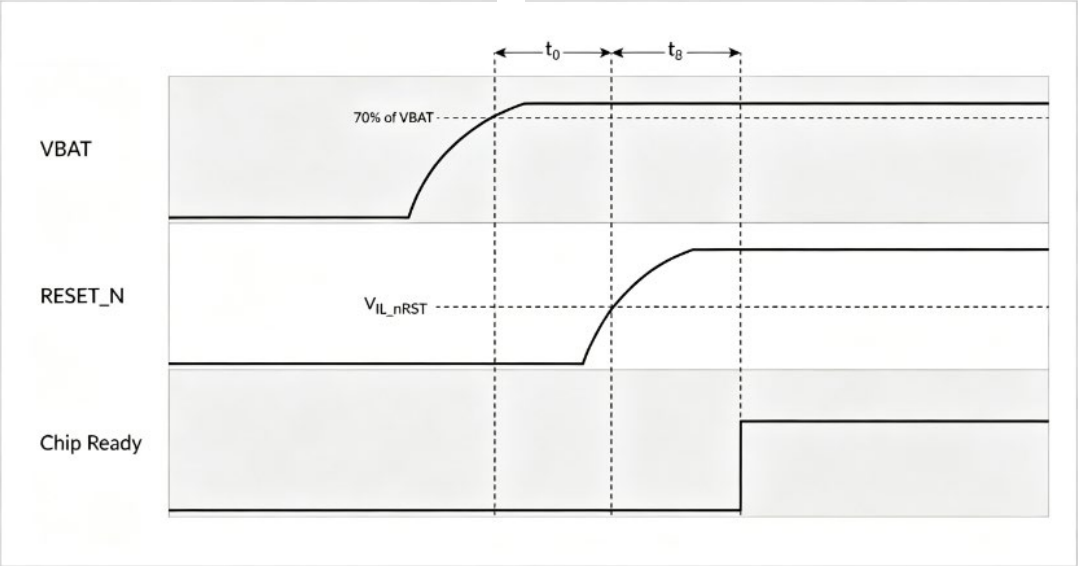
Recommended SPI host interface circuit using power-saving features



Recommended SPI host interface circuit for always-on applications

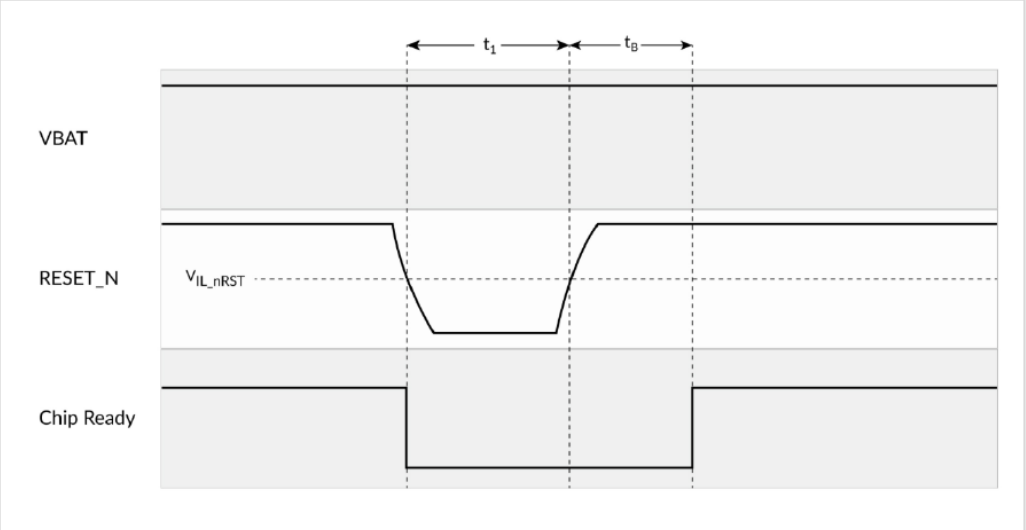
2.4 Timing Sequence

■ Boot Timing



Parameter	Description	Min.	Max.	Unit
VIL_nRST	Reset threshold	450	-	mV
t0	Time between VBAT brought up (3.3V) and RESET_N being activated	50	-	μs
tB	Boot time	-	10	ms

Reset Timing



Parameter	Description	Min.	Max.	Unit
V_{IL_nRST}	Reset threshold	450	-	mV
t0	Duration of RESET_N signal level < V_{IL_nRST} to reset the chip	1000	-	μs
tB	Boot time	-	10	ms

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Stress beyond absolute maximum ratings may cause permanent damage to the module. Functional operation is guaranteed for recommended operation conditions only. Operation of the device outside of recommended conditions may result in reduced lifetime and/or reliability problems even if the absolute maximum ratings are not exceeded.

Parameter	Min.	Max.	Unit
VBAT	-0.3	3.6	V
RESET_N/WAKE_UP	-0.3	3.6	V
Digital I/O pin	-0.3	VDDIO + 0.3	V
Analog	-0.3	1.2	V

3.2 ESD Immunity

Parameter			Min.	Max.	Unit
Electrostatic Discharge (ESD) Performance	Charged device model (CDM), per JESD22-C101	All pins	-500	500	V

3.3 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient temperature	-40	-	85	℃
Storage temperature	-40	-	125	℃
VBAT	3.0	3.3	3.6	V
VDDIO	2.25	3.3	3.6	V

Unless otherwise specified, performance specifications are achieved under typical operating conditions.

3.4 Current Consumption

Transmit Current Consumption

Mode	Transmit Power at Filter Output T_A=25℃, V_{BAT}=V_{DDIO}=3.3V (dBm)	V_{BAT} Current	Unit
1/2/4/8MHz channel, 100% duty cycle OFDM	23	200	mA
	21	145	mA
	19	115	mA
	17	95	mA

Receive Current Consumption

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	V_{BAT} Current	Unit
Listen	2MHz channel bandwidth	19	mA
Active receive	2MHz channel bandwidth	20	mA

Sleep Current Consumption

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	V_{BAT} Current	V_{DDIO} Current	Unit
Snooze	RTC On, >72kB SRAM retained, wake on timer, external IRQ or USB resume	<20	<1	μA
Deep sleep	RTC on, wake on timer or external IRQ	2	<1	μA
Hibernate	RTC off, wake on RESET_N toggle	1	<1	μA

Standby Associated Current

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	Average V_{BAT} Current	Unit
DTIM3	2MHz channel, RTC=RC oscillator	230	μA
DTIM10	2MHz channel, RTC=RC oscillator	103	μA
DTIM3	2MHz channel, RTC=RTC_XTAL	215	μA
DTIM10	2MHz channel, RTC=RTC_XTAL	77	μA

3.5 RF Specifications

Frequency Range

The module operates in the frequency range from 850MHz to 950MHz. The following table shows the primary regulatory environments that the module is designed to work in.

Region	Sub-1GHz Bands	Total BW Available in Each Regulatory Domain
USA	902-928MHz	26MHz
Europe	863-868MHz, 916.4-919.4MHz	8MHz
Australia	915-928 MHz	13MHz
South Korea	917.5-923.5MHz, 926-930MHz	10MHz
Japan	920.5-921.5MHz, 922.5-927.5MHz	6MHz
Singapore	866-869MHz, 920-925MHz	8MHz

Receiver

- Sensitivity

Sensitivities for 10% packet error rate, 256-byte packets:

MCS Index	Modulation Scheme	Coding Rate	Phy Rate (kbps) per BW				Minimum Receive Sensitivity (dBm)			
			1MHz	2MHz	4MHz	8MHz	1MHz	2MHz	4MHz	8MHz
0	BPSK	1/2	333	722	1500	3250	-106	-103	-102	-97
1	QPSK	1/2	667	1444	3000	6500	-105	-102	-99	-94
2	QPSK	3/4	1000	2167	4500	9750	-102	-99	-96	-92
3	16-QAM	1/2	1333	2889	6000	13000	-99	-96	-94	-90
4	16-QAM	3/4	2000	4333	9000	19500	-96	-93	-90	-87
5	64-QAM	2/3	2667	5778	12000	26000	-92	-89	-86	-83
6	64-QAM	3/4	3000	6500	13500	29250	-91	-88	-85	-80
7	64-QAM	5/6	3333	7222	15000	32500	-89	-86	-83	-79
8	256-QAM	3/4	4000	8667	18000	39000	-85	-82	-79	-75
9	256-QAM	5/6	4444	N/A	20000	43333	-83	N/A	-77	-73
10	BPSK	1/2 x 2	167	N/A			-109	N/A		

- Adjacent Channel Rejection

Adjacent channel rejection is measured by setting the requested signal's strength 3dB above the rate dependent sensitivity specified above and raising the power of the interfering signal until 10% PER is caused for a PSDU length of 256-byte packets. The power difference between the interfering and requested channel is the corresponding adjacent channel rejection:

BW (MHz)	MCS Index	Adjacent Channel Rejection (dB) IEEE Spec	Adjacent Channel Rejection (dB)
1	0	16	27
	7	-2	3
2	0	16	26
	7	-2	2
4	0	16	25
	7	-2	1
8	0	16	25
	7	-2	1

- Transmitter

MCS Index	Tx Average Power at Filter Output (dBm) per BW T_A=25℃, V_{BAT}=V_{DDIO}=3.3V, SEM & FCC Compliant			
	1MHz	2MHz	4MHz	8MHz
0	23	23	22	20
1	23	23	22	20
2	23	23	22	20
3	23	23	22	20
4	22	23	22	20
5	21	22	22	20
6	20	21	21	20
7	19	20	20	20
8	17	18	18	18
9	15	N/A	17	17
10	23	N/A	N/A	N/A

4. Ordering Information

Ordering No.	SoC	Main I/O	Operating Temp.	SW
VT-MOB-AH-8108	Morse Micro MM8108	GPIO, SDIO/SPI, USB, JTAG	-40℃ ~ +85℃	-

Packing List	
VT-MOB-AH-8108 Wi-Fi HaLow module	1