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VT-MOB-AH-8108 Wi-Fi HaLow Module

1. Overview

1.1 Product Brief

VT-MOB-AH-8108 is an LGA packaged Wi-Fi HaLow module based on Morse Micro's MM8108 single-chip SoC, which includes radio, PHY, and MAC sections designed to comply with IEEE 802.11ah standard. The standard provides support for operation in the sub 1GHz license exempt RF bands, providing ultra-long-range and low-power wireless connectivity.

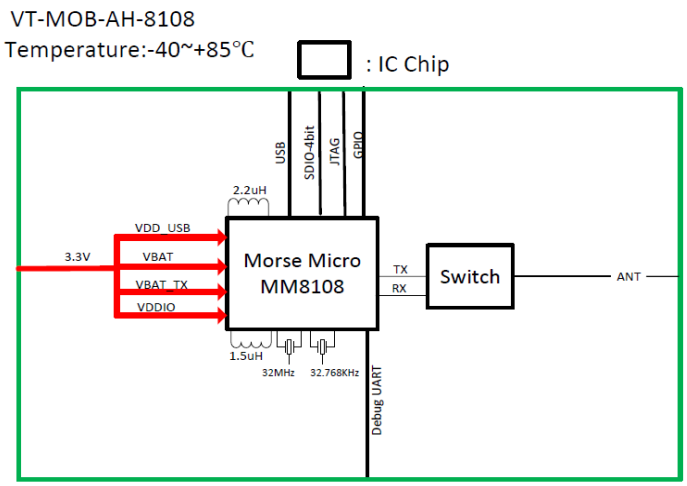
VT-MOB-AH-8108 supports single-stream data rates of up to 43.3 Mbps at the 8MHz bandwidth. It provides USB 2.0, SDIO 2.0/SPI device interfaces, and its MAC supports both station (STA) and access point (AP) role. The module is built with robust security features, including WPA3 encryption, and delivers optimal performance, thanks to its integrated power amplifier (PA), low-noise amplifier (LNA), and transmit/receive (T/R) switch.

VT-MOB-AH-8108 can be easily integrated to IoT communication devices to allow users to quickly build their own Wi-Fi HaLow solutions, such as industrial IoT, smart agriculture, and large-scale sensor networks.

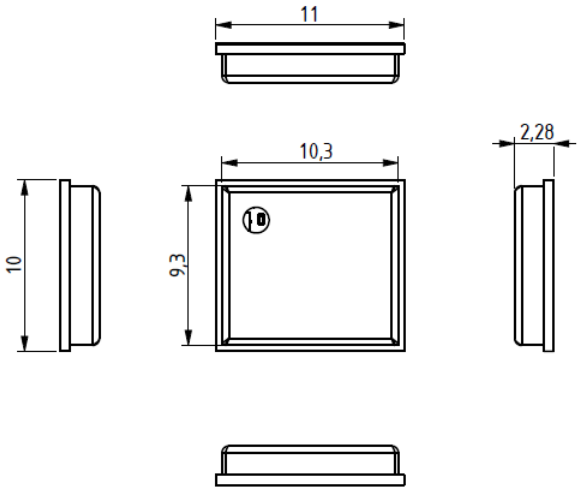
1.2 Features

- Single-stream data rate up to 43.3Mbps at 8MHz channel bandwidth
- Support worldwide Sub-1GHz frequency bands
  - Frequency range: 850MHz~950MHz
  - Channel bandwidth options: 1/2/4/8MHz
  - Max. output power: 23dBm (200mW) at 40% PA efficiency and 30% whole SoC efficiency
  - Ultra-low power receiver with integrated LNA, NF < 4dB
  - Compatible with external LNA, PA for higher power or sensitivity requirements
- 802.11ah MAC capable of WFA Wi-Fi HaLow certification
  - Support both STA and AP roles
  - Listen-Before-Talk (LBT) access with energy detect
  - 802.11 power saving
  - 802.11 fragmentation and defragmentation
  - Power-Saving Target Wake Time (TWT) support for long battery life
  - Automatic and manual MCS rate selection
- Software stack with host offload for Wi-Fi connection management
- Power Management Unit (PMU) supporting various modes of operation
- Wide spectrum of security features
  - Wi-Fi layer security including WPA3, protected management frames (PMF) and Opportunistic Wireless Encryption (OWE)
  - Hardware support for AES and SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- SDIO 2.0 compliant slave interface
  - SDIO 2.0 High-Speed at 50MHz max for 200Mbps
  - Support 1-bit and 4-bit data modes
  - Support SPI mode operation at up to 80MHz for 80Mbps
- USB 2.0 High-Speed device interface supporting up to 480Mbps
- 802.11ah OFDM PHY supporting WFA Wi-Fi HaLow certification
  - BPSK, QPSK, 16-QAM, 64-QAM & 256-QAM modulation
  - Automatic frequency & gain control
  - Packet detection & channel equalization
  - Forward Error Correction (FEC) coding & decoding
  - Support Modulation and Coding Scheme (MCS) levels 0-10
  - Support 1 MHz duplicate mode
  - Support optional traveling pilot

1.3 Block Diagram



1.4 Product Outlines



1.5 Applications

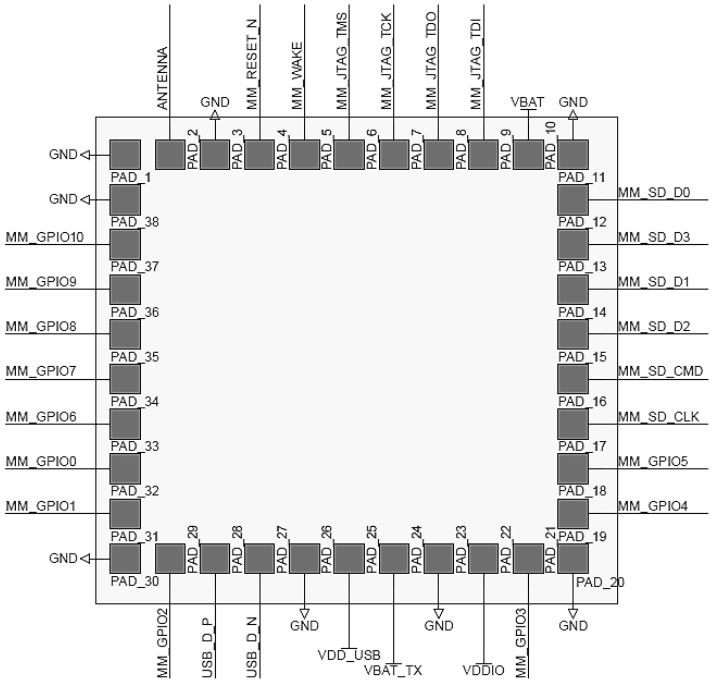
- Home Automation
  - Surveillance cameras, smart doorbells
  - Entertainment (media streaming adapters, speakers)
  - Baby monitors
  - Garage door openers
  - Door locks
  - Smart appliances
  - Energy management
  - Voice control frontends
  - Consumer robotics
- Portables & Wearables
  - Smart watches
  - Smart glasses
  - Health trackers
  - Low-power sensor networks
- Smart Building
  - Building access control & security
  - HVAC & air quality control
  - Smart city networks
  - Commercial robotics
  - EV battery charger
  - Vehicle firmware OTA update
- Retail & Logistics
  - Digital signage
  - Kiosks / POS / vending machine
  - Fleet management
  - Inventory management / scanners
- Industrial Automation
  - Autonomous mobile robotics
  - Material handlers / trackers

1.6 Specifications

VT-MOB-AH-8108					
Major Chipset	Morse Micro MM8108 HaLow SoC				
I/O	Host interface	1 x USB 2.0 (Device)			
		1 x 1-bit/4-bit SDIO (combo with SPI)			
	GPIO	13 x GPIO			
	JTAG	Supported			
WLAN Features	Wi-Fi standard	IEEE 802. 11ah			
	Frequency range (Sub 1 GHz bands)	850MHz ~ 950MHz			
	Channel bandwidth	1 / 2 / 4 /8MHz			
	Data rate* (256-QAM)	1MHz	2MHz	4MHz	8MHz
		4.44Mbps (Max.)	8.67Mbps (Max.)	20Mbps (Max.)	43.3Mbps (Max.)
	Security	AES encryption engine			
		SHA1 and SHA2 hash algorithms (SHA-256, SHA-384, SHA-512)			
		WPA3			
		Protected management frames (PMF)			
		Opportunistic Wireless Encryption (OWE)			
Mechanical	Dimensions	11mm x 10mm x 2.28mm			
	Power	3.3V/1A DC input			
	Temperature	Operating: -40℃~+85℃		Storage: -40℃~+85℃	
	Humidity	Less than 85% (Non-condensing)			
	Packaging	LGA			

* These represent theoretical maximum values for the 256-QAM modulation scheme.

1.7 Pinout



Pin	Name	Type	Primary function	Alternate function
1	GND	Power	Ground	
2	Antenna	I/O	Antenna	
3	GND	Power	Ground	
4	MM_RESET_N	Analog	System Reset (active low)	
5	MM_WAKE	Analog	External input wake from Deep Sleep and Snooze modes	
6	MM_JTAG_TMS	I	JTAG Test Mode Select	
7	MM_JTAG_TCK	I	JTAG Test Clock	
8	MM_JTAG_TDO	O	JTAG Test Data Out	
9	MM_JTAG_TDI	I	JTAG Test Data Input	
10	VBAT	Power	3.3V VBAT Supply	
11	GND	Power	Ground	
12	MM_SD_D0	I/O	SDIO Data 0	SPI_MISO
13	MM_SD_D3	I/O	SDIO Data 3	SPI_CS (active low)
14	MM_SD_D1	I/O	SDIO Data 1	
15	MM_SD_D2	I/O	SDIO Data 2	
16	MM_SD_CMD	I/O	SDIO Command	SPI_MOSI
17	MM_SD_CLK	I/O	SDIO Clock	SPI_SCK
18	MM_GPIO5	I/O	GPIO5	
19	MM_GPIO4	I/O	GPIO4	
20	GND	Power	Ground	

Pin	Name	Type	Primary function	Other function
21	MM_GPIO3	I/O	GPIO3	
22	VDDIO	Power	3.3V VDD Supply for Digital I/O	
23	GND	Power	Ground	
24	VBAT_TX	Power	3.3V VBAT Supply	
25	VDD_USB	Power	3.3V Analog Supply Voltage for USB 2.0	
26	GND	Power	Ground	
27	USB_D_M	I/O	USB differential data line -	
28	USB_D_P	I/O	USB differential data line +	
29	MM_GPIO2	I/O	GPIO2	
30	GND	Power	Ground	
31	MM_GPIO1	I/O	GPIO1	
32	MM_GPIO0	I/O	GPIO0	
33	MM_GPIO6	I/O	GPIO6	
34	MM_GPIO7	I/O	GPIO7	
35	MM_GPIO8	I/O	GPIO8	
36	MM_GPIO9	I/O	GPIO9	
37	MM_GPIO10	I/O	GPIO10	
38	GND	Power	Ground	

2. System Design

2.1 Power Management

The power for VT-MOB-AH-8108 is derived from a 3V to 3.6V VBAT supply connected to pins VBAT and VBAT_TX as input power rails to the internal buck DC-DC converters.

There is one digital LDO regulator that generates various digital supply rails by passing through independently controlled power switches. There is also a low-power LDO regulator that takes VBAT as its input and generates a retention voltage for sleeping modes.

2.2 Digital Interfaces

VT-MOB-AH-8108 implements a host interface that operates at 3.3V. After power-on, this host interface can be brought up as either SDIO or SPI. Please refer to 2.3 Recommended Usage Schematics for the configuration of SDIO/SPI.

■ SDIO Device

The SDIO 2.0 interface supports both 1-bit and 4-bit data modes, with data rates up to 200Mbps at 50MHz.

Pin Name	SDIO 4-Bit Mode	SDIO 1-Bit Mode
MM_SD_CLK	Clock pin (input)	
MM_SD_CMD	Command pin	
MM_SD_D0	Data pin 0	
MM_SD_D1	Data pin 1	IRQ
MM_SD_D2	Data pin 2	Unused
MM_SD_D3	Data pin 3	Unused

- Unused pins should be pulled high.

■ SPI Device

The SPI master interface uses the physical unidirectional pin layout as defined below, over which the modified SDIO protocol is used for communication. As per the SDIO specification, to switch the interface to SPI mode, the host must send a CMD0 while holding CS low (its asserted state).

Pin Name	SPI Mode Function
MM_SD_CLK	Clock pin (input)
MM_SD_D3	Chip select (active low)
MM_SD_CMD	Master data out/slave data in
MM_SD_D0	Master data in/slave data out
MM_SD_D1	Not connected/unused (tie high)
MM_SD_D2	Not connected/unused (tie high)

GPIO

The GPIO hardware consists of a register to set each pin's drive enable, drive value and read the value present on the pin (whether driving or not).

Each pin can also be configured to generate an interrupt based on level, or edge (rising or falling). Each pin can be an individual interrupt source via the platform interrupt controller. Inputs are synchronized to the main digital clock and so any pulses must be at least 3 x 96MHz clock cycles in length.

There are internal pull-up and pull-down facilities in the pads, as well as drive-strength selection.

At cold boot GPIOs will be undriven and in a high-impedance state. During power-save, the GPIOs can be programmed to retain their output state.

USB

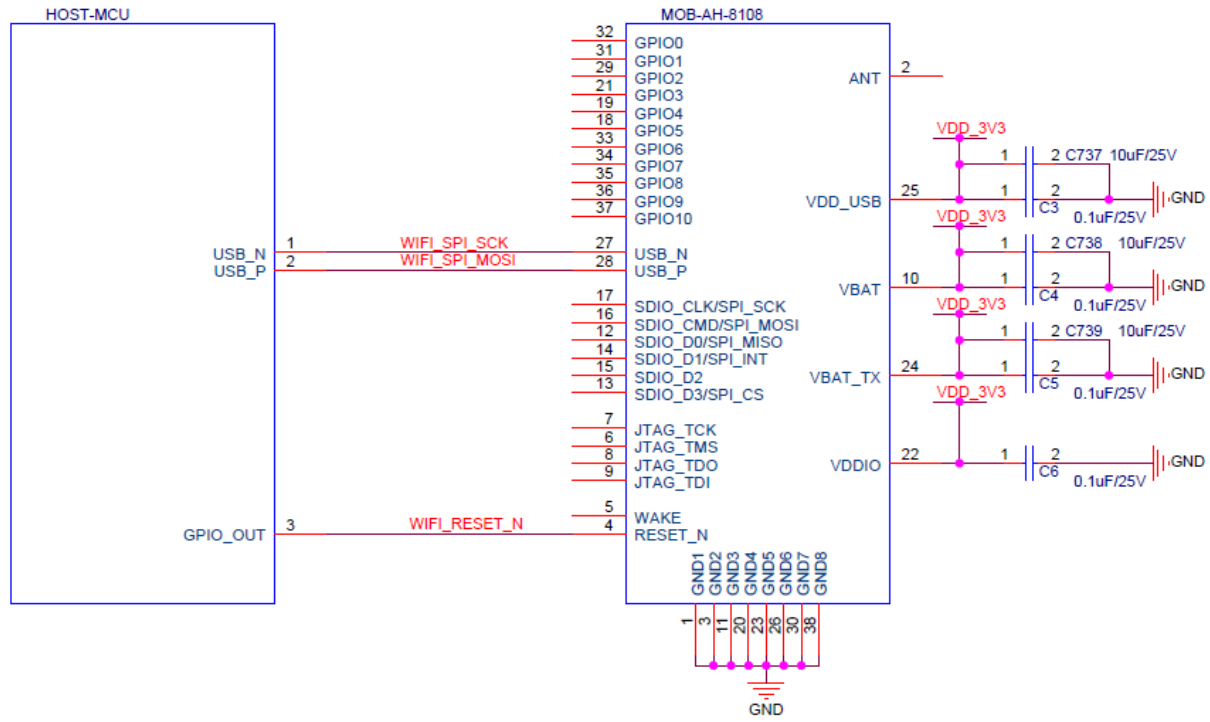
The USB 2.0 interface supports device mode only at up to 480Mbps, providing a high throughput host interface.

Pin Name	SPI Mode Function
USB_D_P	High speed differential pin, DP
USB_D_M	High speed differential pin, DM
VDD_USB	3.3V analog supply voltage for USB 2.0

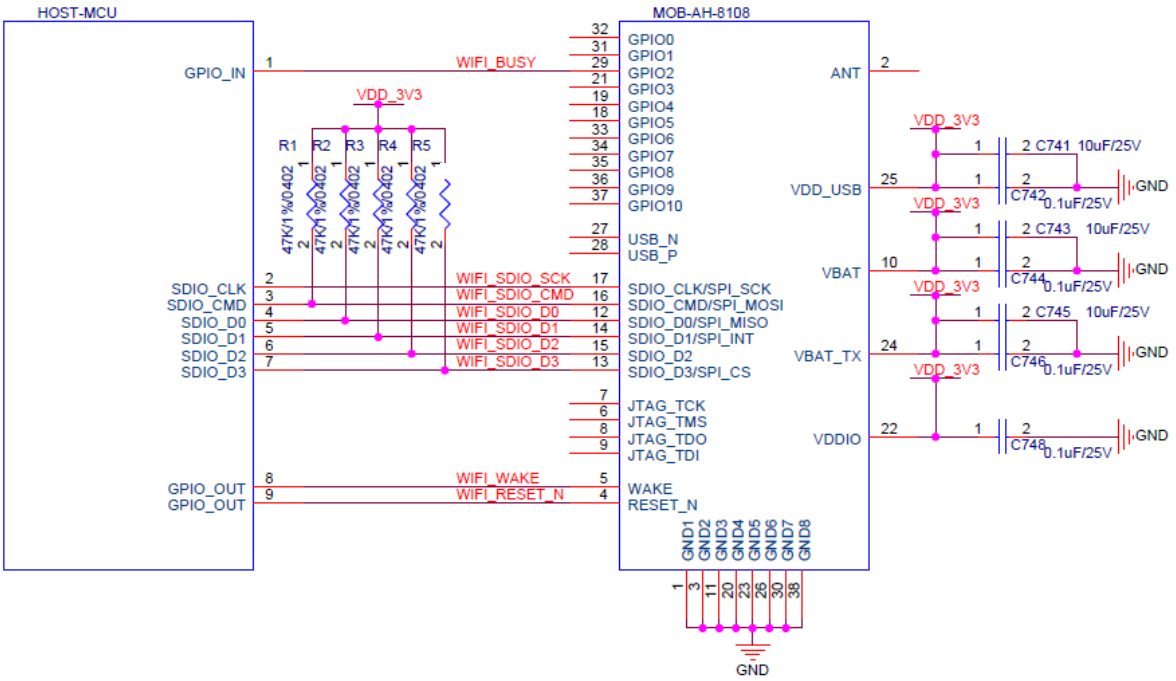
- USB 2.0 PHY and MAC capable of up to High-Speed mode at 480Mbps.
- Device endpoints implementing bulk data, isochronous transfers and interrupts sufficient for USB host driver to operate chip as network AP or STA
- Suspend and resume power management functions
- USB snooze mode with in-band wake:
  - Snooze mode is a low power mode the chip may enter and return from with full state retention
  - To enter USB snooze, the USB link must be in suspend state
  - USB host issuing resume signaling over the USB bus (ie. in-band) will initiate chip wake from USB snooze and return to continuation of operation

Parameter	Min.	Typ.	Max.	Unit
VDD_USB	0.3	3.3	3.6	V
V_{noise_33A} (Allowable power noise on supply, 1Hz-1kHz)	-	-	150	V
I_{VCC33A} in High-Speed mode (480Mbps)	-	8.1	8.4	V

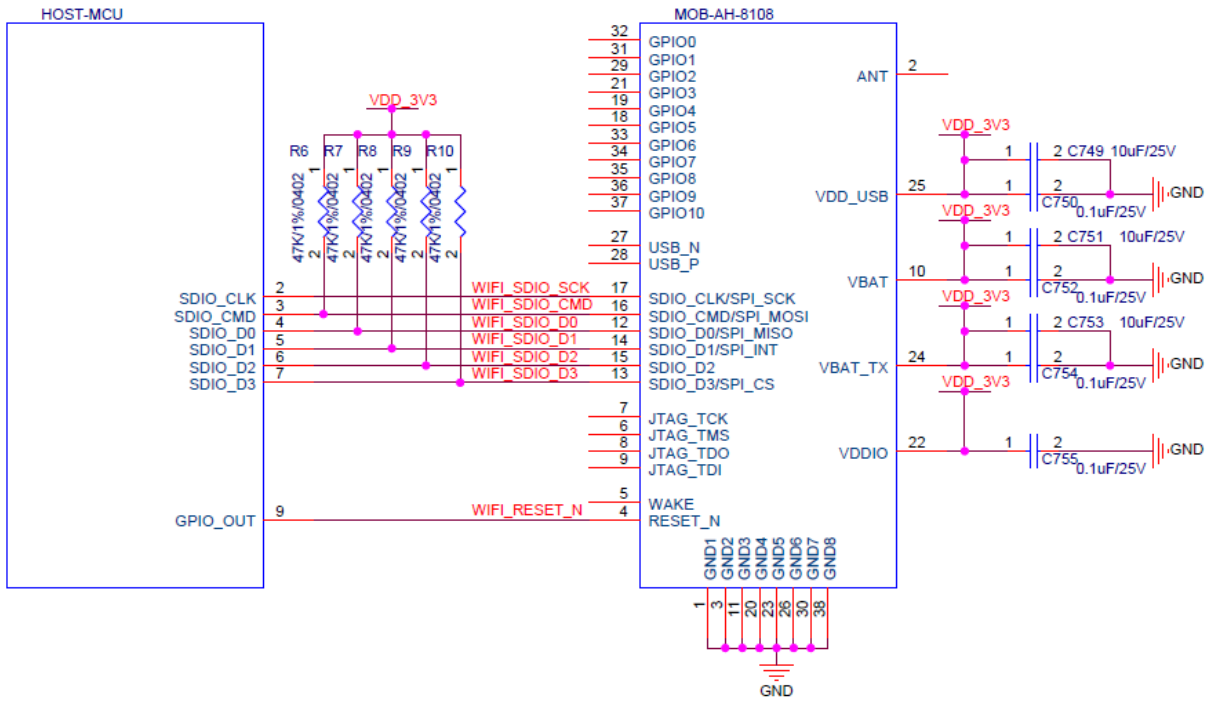
2.3 Recommended Usage Schematics



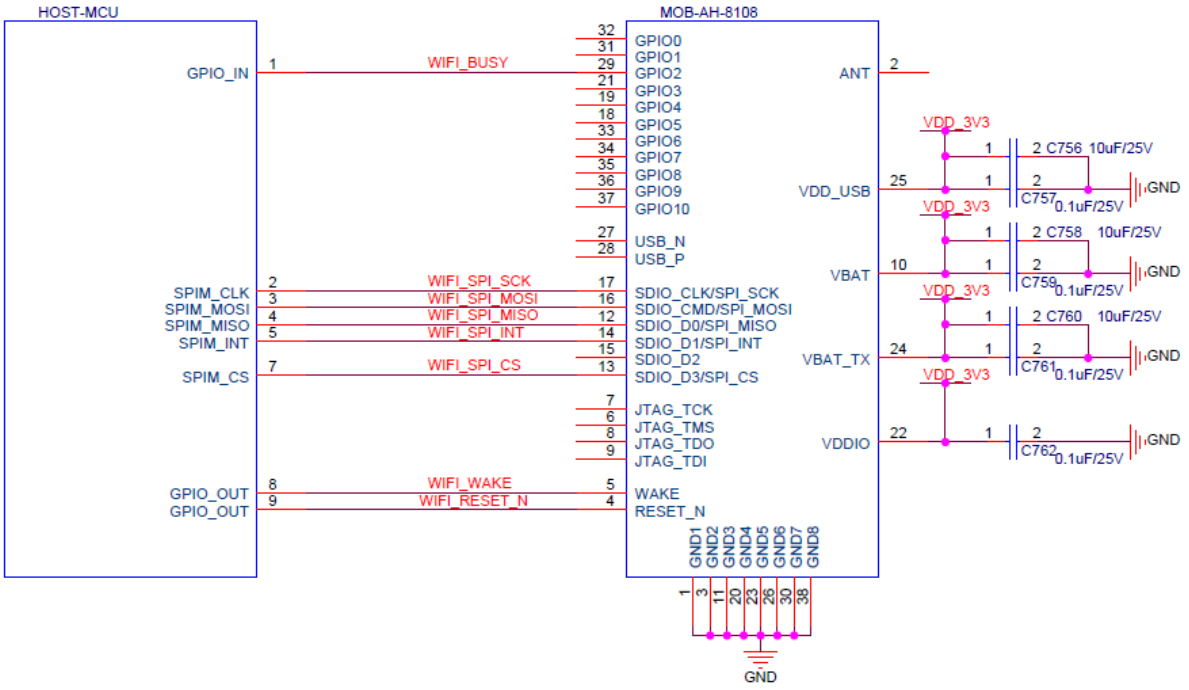
Recommended USB host interface circuit



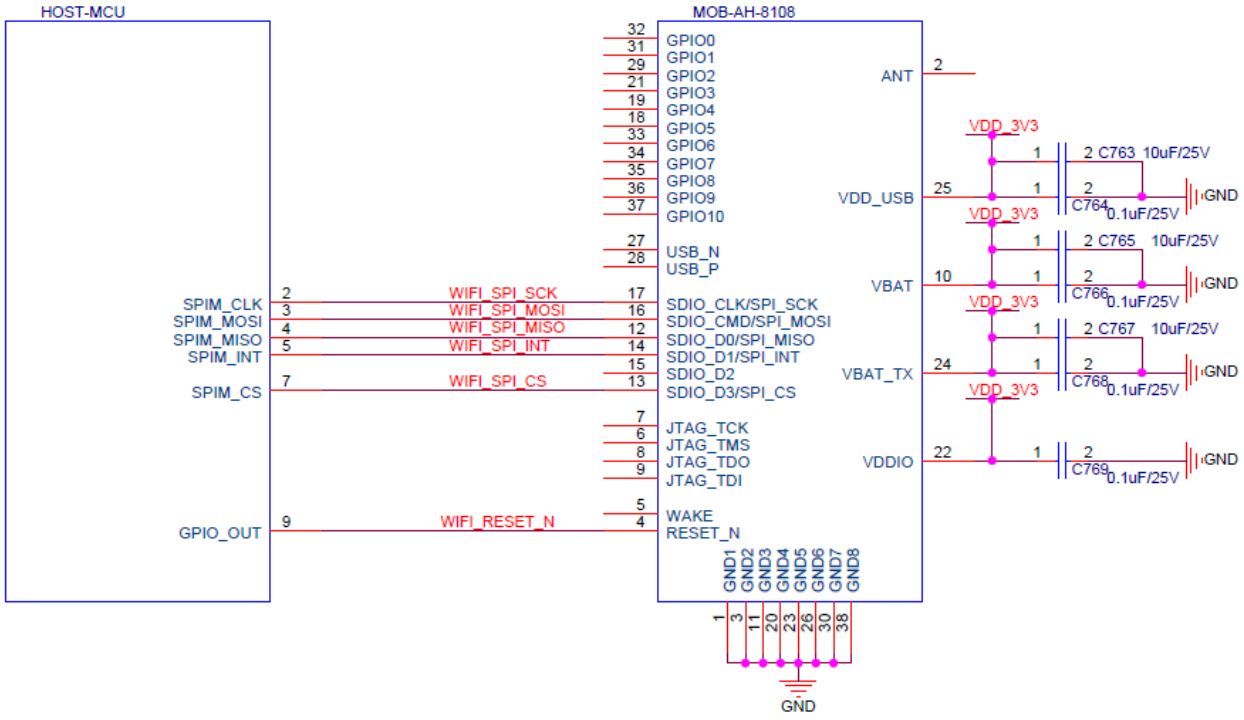
Recommended SDIO host interface circuit using power-saving features



Recommended SDIO host interface circuit for always-on applications



Recommended SPI host interface circuit using power-saving features

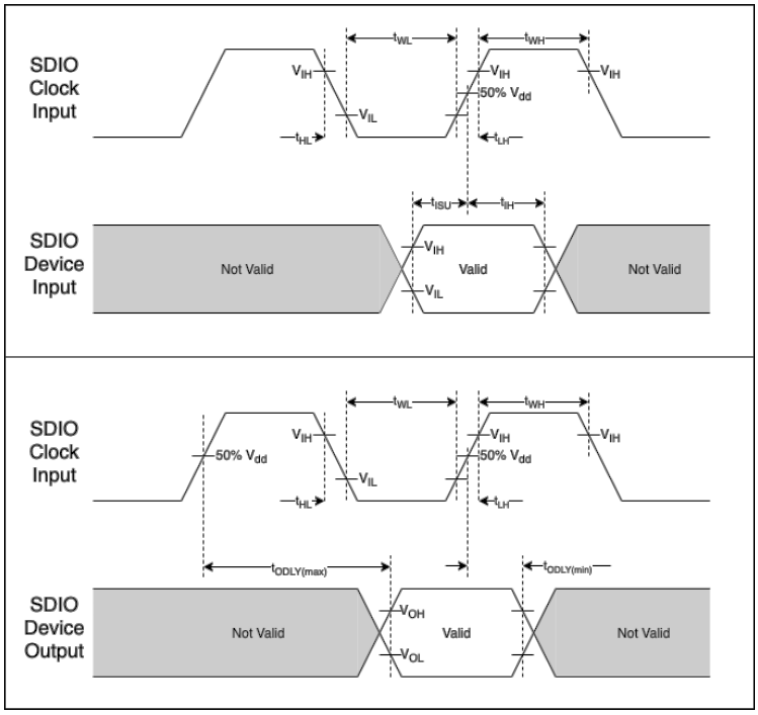


Recommended SPI host interface circuit for always-on applications

2.4 Timing Sequence

■ SDIO bus timing

The SDIO interface supports a clock rate up to 50MHz. The device always operates in SD bus High-Speed mode.



Parameter	Min.	Max.
Clock parameters		
Clock frequency	0 MHz	50 MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT Lines to Device from Host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT Lines from Device to Host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

■ SPI bus timing

The SPI interface supports a clock rate up to 80MHz. The SPI bus timing is **identical to the SDIO bus timing**, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge) after being initialized.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Stress beyond absolute maximum ratings may cause permanent damage to the module. Functional operation is guaranteed for recommended operation conditions only. Operation of the device outside of recommended conditions may result in reduced lifetime and/or reliability problems even if the absolute maximum ratings are not exceeded.

Parameter	Min.	Max.	Unit
VBAT	-0.3	3.6	V
RESET_N/WAKE_UP	-0.3	3.6	V
Digital I/O pin	-0.3	VDDIO + 0.3	V
Analog	-0.3	1.2	V

3.2 Immunity

Parameter			Min.	Max.	Unit
Electrostatic Discharge (ESD) Performance	Charged device model (CDM), per JESD22-C101	All pins	-500	500	V

3.3 Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient temperature	-40	-	85	℃
Storage temperature	-40	-	125	℃
VBAT	3.0	3.3	3.6	V
VDDIO	2.25	3.3	3.6	V

Unless otherwise specified, performance specifications are achieved under typical operating conditions.

3.4 Current Consumption

Transmit Current Consumption

Mode	Transmit Power at Filter Output T_A=25℃, V_{BAT}=V_{DDIO}=3.3V (dBm)	V_{BAT} Current	Unit
1/2/4/8MHz channel, 100% duty cycle OFDM	23	200	mA
	21	145	mA
	19	115	mA
	17	95	mA

Receive Current Consumption

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	V_{BAT} Current	Unit
Listen	2MHz channel bandwidth	19	mA
Active receive	2MHz channel bandwidth	20	mA

Sleep Current Consumption

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	V_{BAT} Current	V_{DDIO} Current	Unit
Snooze	RTC On, >72kB SRAM retained, wake on timer, external IRQ or USB resume	<20	<1	μA
Deep sleep	RTC on, wake on timer or external IRQ	2	<1	μA
Hibernate	RTC off, wake on RESET_N toggle	1	<1	μA

Standby Associated Current

Mode	Condition T_A=25℃, V_{BAT}=V_{DDIO}=3.3V	Average V_{BAT} Current	Unit
DTIM3	2MHz channel, RTC=RC oscillator	230	μA
DTIM10	2MHz channel, RTC=RC oscillator	103	μA
DTIM3	2MHz channel, RTC=RTC_XTAL	215	μA
DTIM10	2MHz channel, RTC=RTC_XTAL	77	μA

3.5 RF Specifications

Frequency Range

The module operates in the frequency range from 850MHz to 950MHz. The following table shows the primary regulatory environments that the module is designed to work in.

Region	Sub-1GHz Bands	Total BW Available in Each Regulatory Domain
USA	902-928MHz	26MHz
Europe	863-868MHz, 916.4-919.4MHz	8MHz
Australia	915-928 MHz	13MHz
South Korea	917.5-923.5MHz, 926-930MHz	10MHz
Japan	920.5-921.5MHz, 922.5-927.5MHz	6MHz
Singapore	866-869MHz, 920-925MHz	8MHz

Receiver

- Sensitivity

Sensitivities for 10% packet error rate, 256-byte packets:

MCS Index	Modulation Scheme	Coding Rate	Phy Rate (kbps) per BW				Minimum Receive Sensitivity (dBm)			
			1MHz	2MHz	4MHz	8MHz	1MHz	2MHz	4MHz	8MHz
0	BPSK	1/2	333	722	1500	3250	-106	-103	-102	-97
1	QPSK	1/2	667	1444	3000	6500	-105	-102	-99	-94
2	QPSK	3/4	1000	2167	4500	9750	-102	-99	-96	-92
3	16-QAM	1/2	1333	2889	6000	13000	-99	-96	-94	-90
4	16-QAM	3/4	2000	4333	9000	19500	-96	-93	-90	-87
5	64-QAM	2/3	2667	5778	12000	26000	-92	-89	-86	-83
6	64-QAM	3/4	3000	6500	13500	29250	-91	-88	-85	-80
7	64-QAM	5/6	3333	7222	15000	32500	-89	-86	-83	-79
8	256-QAM	3/4	4000	8667	18000	39000	-85	-82	-79	-75
9	256-QAM	5/6	4444	N/A	20000	43333	-83	N/A	-77	-73
10	BPSK	1/2 x 2	167	N/A			-109	N/A		

- Adjacent Channel Rejection

Adjacent channel rejection is measured by setting the requested signal's strength 3dB above the rate dependent sensitivity specified above and raising the power of the interfering signal until 10% PER is caused for a PSDU length of 256-byte packets. The power difference between the interfering and requested channel is the corresponding adjacent channel rejection:

BW (MHz)	MCS Index	Adjacent Channel Rejection (dB) IEEE Spec	Adjacent Channel Rejection (dB)
1	0	16	27
	7	-2	3
2	0	16	26
	7	-2	2
4	0	16	25
	7	-2	1
8	0	16	25
	7	-2	1

- Transmitter

MCS Index	Tx Average Power at Filter Output (dBm) per BW T_A=25℃, V_{BAT}=V_{DDIO}=3.3V, SEM & FCC Compliant			
	1MHz	2MHz	4MHz	8MHz
0	23	23	22	20
1	23	23	22	20
2	23	23	22	20
3	23	23	22	20
4	22	23	22	20
5	21	22	22	20
6	20	21	21	20
7	19	20	20	20
8	17	18	18	18
9	15	N/A	17	17
10	23	N/A	N/A	N/A

4. Ordering Information

Ordering No.	SoC	Main I/O	Operating Temp.	SW
VT-MOB-AH-8108	Morse Micro MM8108	GPIO, SDIO/SPI, USB, JTAG	-40℃ ~ +85℃	-

Packing list	
VT-MOB-AH-8108 Wi-Fi HaLow module	1

5. Company Profile

Since its establishment in 2002 by two Silicon Valley entrepreneurs, Vantron Technology has been at the forefront of the connected IoT devices and IoT platform solutions. Today, Vantron boasts a global customer base that includes several Fortune 500 companies. Its product lines cover edge intelligent hardware, IoT communication devices, industrial displays and BlueSphere cloud device management platforms.

With over 20 years of experience in R&D of embedded edge intelligent hardware, Vantron has provided users with diverse embedded solutions featuring ARM and X86 architectures. Its offerings range from Linux to Windows, from embedded to desktop level, and from gateway to server. In addition, it provides users with system clipping, driver transplantation and other related services.

Vantron's IoT communication devices support multi-protocol connections for industrial equipment and local data edge computing. Offering a range of wired and wireless connectivity options, these devices enable remote operations and maintenance across various sectors, from electricity and transportation to smart retail, medical, and warehousing. Vantron's IoT solutions are designed to facilitate digital transformation for many companies, leading to significant improvements in manufacturing efficiency and productivity.

Vantron's intelligent display systems encompass a range of cutting-edge devices, designed to elevate device performance and deliver exceptional human-machine interactive experiences. Equipped with industry-leading brands like Rockchip, NXP, MediaTek, and Intel, such devices offer powerful performance and versatility. They provide flexible installation options to suit diverse application scenarios. Additionally, they are engineered to thrive in challenging environments, boasting advanced features such as waterproofing, dustproofing, and shatter resistance for optimal durability and performance.

Vantron BlueSphere device management platforms, a suit of cloud-based PaaS solutions, are playing a pivotal role in Vantron's overall IoT offerings. Today, Vantron remains committed to providing cost-effective, cutting-edge, and reliable solutions, empowering customers to realize their visions with confidence.