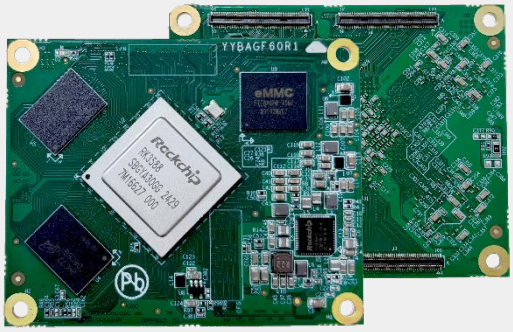
VT-CORE-3588

Computer-on-Module



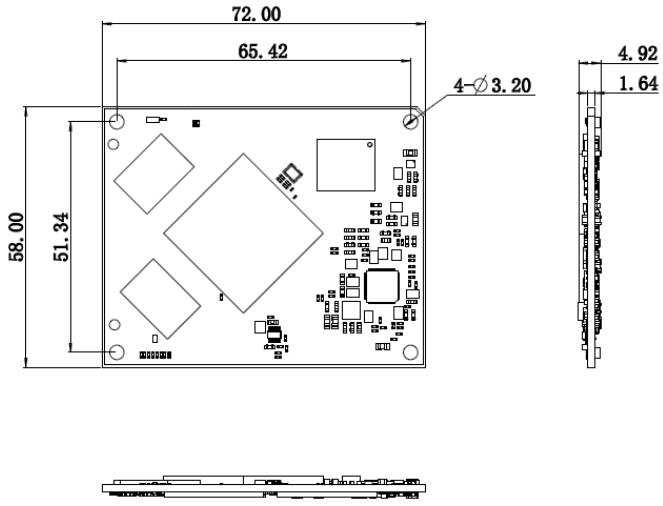
Product Brief

VT-CORE-3588 computer-on-module is powered by Rockchip's flagship RK3588 AIoT chipset, seamlessly integrating high-performance computing, and advanced multimedia capabilities within a compact and energy-efficient form factor. It features an octa-core 64-bit CPU and a powerful ARM Mali-G610 MP4 GPU, delivering seamless multitasking and advanced graphics rendering. The 6 TOPS built-in NPU excels in machine learning and AI workloads, making it ideal for applications such as smart vision, robotics, and edge AI.

VT-CORE-3588 supports 8K video decoding, 8K encoding, and multiple display outputs, enabling stunning visuals for digital signage, smart displays, and multimedia systems. In addition, it offers rich I/O options, including MIPI DSI, MIPI CSI, HDMI, USB, CAN, I^2C, PCIe, and UART, all routed to four expansion headers for flexible integration and scalability.

Designed as a reliable and versatile industrial IoT solution, VT-CORE-3588 is perfect for AI-driven IoT devices, robotics, multimedia entertainment, and smart display applications, offering both performance and flexibility in demanding environments.

Product Outlines and Features



VT-CORE-3588
Rockchip RK3588 octa-core flagship processor
8K video decoding and encoding
HDMI/eDP/MIPI DSI for high-quality display
Multiple camera interfaces supported
Rich interfaces for flexible expansion
Dual gigabit Ethernet
AI acceleration and edge computing
Compact and scalable

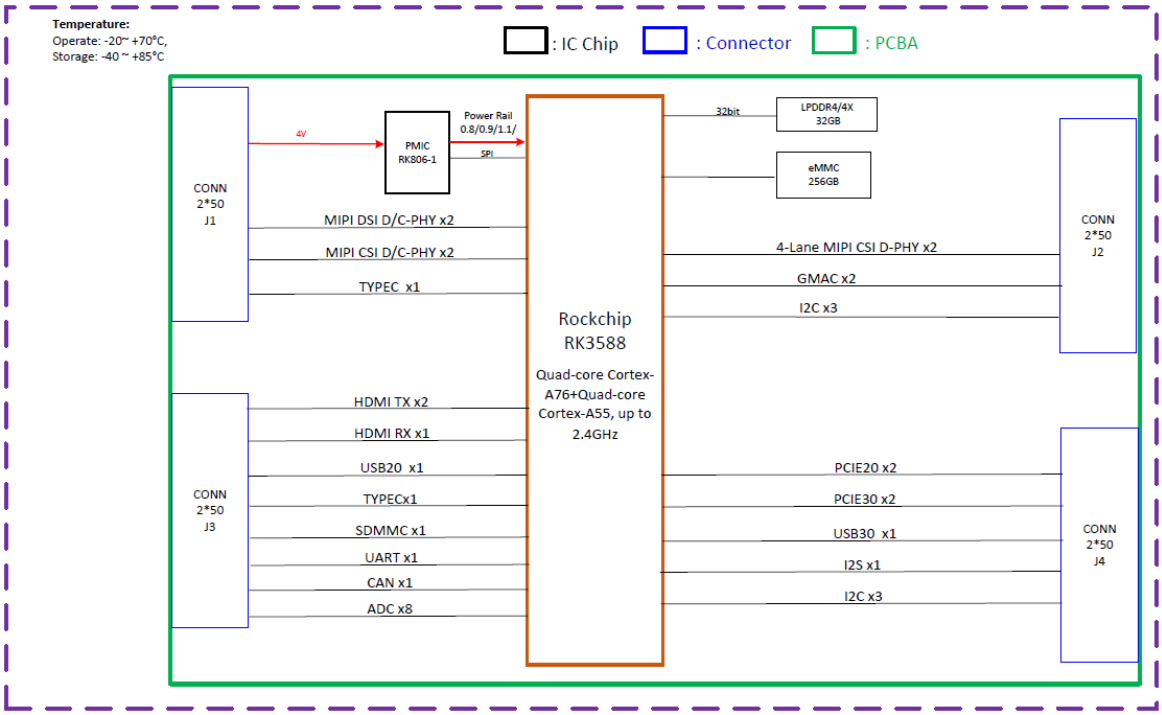
VT-CORE-3588 Computer-on-Module Datasheet

Specifications			
System	CPU	RK3588 Quad-core Cortex-A76 + Quad-core Cortex-A55 processor, Max. 2.4GHz	
	GPU	ARM Mali-G610 MC4, Max. 1GHz OpenGL ES1.1/2.0/3.2, OpenCL 2.2, Vulkan 1.2 supported	
	NPU	6 TOPS, int4/int8/int16/FP16/BF16/TF32 supported	
	Memory	32GB LPDDR4x	
	Storage	256GB eMMC V5.1	
Media	Video processing	8K@30fps H.265/H.264 video encoder	8K@60fps H.265/8K@30fps H.264 video decoder
	Camera ISP	Up to 48MP: 8064 × 6048@15fps dual ISP (HDR, 3DNR, 2DNR)	
Power	Input	4V DC	
	Consumption	Typical: 1.8W (power-on without applications running)	
Software	Operating system	Android12, Debian 11, Ubuntu 20.04	
	Device management	BlueSphere MDM (Android version optional)	
Mechanical	Dimensions	72mm x 58mm x 4.92mm	
Environment Condition	Temperature	Operating: -20℃ ~ +70℃	Storage: -40℃ ~ +85℃
	Humidity	Operating: 10%~90% RH	Storage: 5%~95% RH

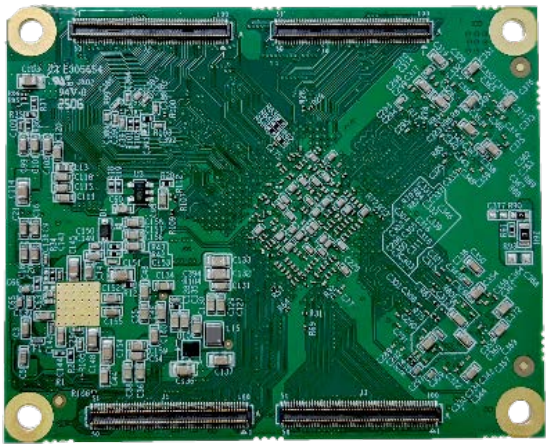
I/O*		
Display	2 x 4-lane MIPI DSI (D-PHY) / 2 x 3-lane MIPI DSI (C-PHY), up to 4K@60Hz	
	2 x HDMI TX 2.0/2.1 / eDP, 7680 × 4320@60Hz for HDMI TX; 4K@60Hz for eDP	
	2 x DP TX 1.4a / USB 3.1 Type-C OTG, up to 7680 × 4320@30Hz	
	1 x HDMI RX 1.4b/2.0, 2160p@60Hz for HDMI 2.0; 1080p@120Hz for HDMI 1.4b	
Camera (4 or 5 or 6 cameras in total)	2 x 4-lane MIPI CSI (D-PHY) / 2 x 3-lane MIPI CSI (C-PHY)	
	2 x 4-lane MIPI CSI (D-PHY) / 4 x 2-lane MIPI CSI (D-PHY) / 1 x 4-lane MIPI CSI + 2 x 2-lane MIPI CSI (D-PHY)	
Ethernet	2 x RGMII/RMII (10/100/1000Mbps)	
USB	2 x USB 3.1 Type-C OTG / DP TX 1.4a	
	1 x USB 3.0 Host	
	1 x USB 2.0 Host	
UART	1 x UART (baud rate up to 4Mbps)	
CAN	1 x CAN (support CAN 2.0B)	
GPIO	124 x GPIO (Max.)	
I^2S	1 x I^2S	
I^2C	6 x I^2C	
PICe	2 x PCIe 2.0 (5Gbps)	2 x PCIe 3.0 (8Gbps)
SATA	1 x SATA 3.0	
ADC	8 x 12-bit SAR-ADC, up to 1MS/S sampling rate	
SDMMC	1 x SDMMC	
PWM	3 x PWM	

* The count of each I/O is based on the default function assigned to the pins, as outlined in **Pinout**.

Block Diagram



Product Exterior



Pinout

Header	Pin	Function 1*	Function 2*	GPIO	Level	Description
J1	100	GND	-	-	-	Ground
	99	TYPEC0_SSRX1_N	DP0_TX0N	-	-	Type-C 0 receiver 1 -
	98	TYPEC0_SSRX1_P	DP0_TX0P	-	-	Type-C 0 receiver 1 +
	97	GND	-	-	-	Ground
	96	TYPEC0_SSTX1_N	DP0_TX1N	-	-	Type-C 0 transmitter 1 -
	95	TYPEC0_SSTX1_P	DP0_TX1P	-	-	Type-C 0 transmitter 1 +

Header	Pin	Function 1*	Function 2*	GPIO	Level	Description
J1	94	GND	-	-	-	Ground
	93	TYPEC0_SSRX2_N	DP0_TX2N	-	-	Type-C 0 receiver 2 -
	92	TYPEC0_SSRX2_P	DP0_TX2P	-	-	Type-C 0 receiver 2 +
	91	GND	-	-	-	Ground
	90	TYPEC0_SSTX2_N	DP0_TX3N	-	-	Type-C 0 transmitter 2 -
	89	TYPEC0_SSTX2_P	DP0_TX3P	-	-	Type-C 0 transmitter 2 +
	88	GND	-	-	-	Ground
	87	MIPI_DPHY1_TX_D0_N	MIPI_CPHY1_TX_TRIO0_A	-	-	MIPI DPHY 1 transmitting data 0 -
	86	MIPI_DPHY1_TX_D0_P	MIPI_CPHY1_TX_TRIO0_B	-	-	MIPI DPHY 1 transmitting data 0 +
	85	GND	-	-	-	Ground
	84	MIPI_DPHY1_TX_D1_N	MIPI_CPHY1_TX_TRIO0_C	-	-	MIPI DPHY 1 transmitting data 1 -
	83	MIPI_DPHY1_TX_D1_P	MIPI_CPHY1_TX_TRIO1_A	-	-	MIPI DPHY 1 transmitting data 1 +
	82	GND	-	-	-	Ground
	81	MIPI_DPHY1_TX_CLK_N	MIPI_CPHY1_TX_TRIO1_B	-	-	MIPI DPHY 1 transmitting clock -
	80	MIPI_DPHY1_TX_CLK_P	MIPI_CPHY1_TX_TRIO1_C	-	-	MIPI DPHY 1 transmitting clock +
	79	GND	-	-	-	Ground
	78	MIPI_DPHY1_TX_D2_N	MIPI_CPHY1_TX_TRIO2_A	-	-	MIPI DPHY 1 transmitting data 2 -
	77	MIPI_DPHY1_TX_D2_P	MIPI_CPHY1_TX_TRIO2_B	-	-	MIPI DPHY 1 transmitting data 2 +
	76	GND	-	-	-	Ground
	75	MIPI_DPHY1_TX_D3_N	MIPI_CPHY1_TX_TRIO2_C	-	-	MIPI DPHY 1 transmitting data 3 -
	74	MIPI_DPHY1_TX_D3_P	-	-	-	MIPI DPHY 1 transmitting data 3 +
	73	GND	-	-	-	Ground
	72	MIPI_DPHY0_TX_D0_N	MIPI_CPHY0_TX_TRIO0_A	-	-	MIPI DPHY 0 transmitting data 0 -
	71	MIPI_DPHY0_TX_D0_P	MIPI_CPHY0_TX_TRIO0_B	-	-	MIPI DPHY 0 transmitting data 0 +
	70	GND	-	-	-	Ground
	69	MIPI_DPHY0_TX_D1_N	MIPI_CPHY0_TX_TRIO0_C	-	-	MIPI DPHY 0 transmitting data 1 -
	68	MIPI_DPHY0_TX_D1_P	MIPI_CPHY0_TX_TRIO1_A	-	-	MIPI DPHY 0 transmitting data 1 +
	67	GND	-	-	-	Ground
	66	MIPI_DPHY0_TX_CLK_N	MIPI_CPHY0_TX_TRIO1_B	-	-	MIPI DPHY 0 transmitting clock -
	65	MIPI_DPHY0_TX_CLK_P	MIPI_CPHY0_TX_TRIO1_C	-	-	MIPI DPHY 0 transmitting clock +
	64	GND	-	-	-	Ground
	63	MIPI_DPHY0_TX_D2_N	MIPI_CPHY0_TX_TRIO2_A	-	-	MIPI DSI 0 transmitting data 2 -
	62	MIPI_DPHY0_TX_D2_P	MIPI_CPHY0_TX_TRIO2_B	-	-	MIPI DSI 0 transmitting data 2 +
	61	GND	-	-	-	Ground
	60	MIPI_DPHY0_TX_D3_N	MIPI_CPHY0_TX_TRIO2_C	-	-	MIPI DPHY 0 transmitting data 3 -
	59	MIPI_DPHY0_TX_D3_P	-	-	-	MIPI DPHY 0 transmitting data 3 +
	58	GND	-			Ground
	57	MIPI_DSI0_RESET	CIF_D3/BT1120_D3/ PCIE30X1_0_CLKREQN_M1/ UART0_TX_M2	GPIO4_A3	3.3V	MIPI DSI 0 reset

* Function 1 is set as the default. For specific pins, there are multiple functions available.

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J1	56	MIPI_DSI1_RESET	CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1	GPIO4_A4	3.3V	MIPI DSI 1 reset
	55	RESET_L	-	-	-	Module reset
	54	VCC4.0	-	-	-	4V power input
	53		-	-	-	4V power input
	52		-	-	-	4V power input
	51		-	-	-	4V power input
	1	GND	-	-	-	Ground
	2	TYPEC1_OTG_D_N	-	-	-	Type-C 1 OTG data -
	3	TYPEC1_OTG_D_P	-	-	-	Type-C 1 OTG data +
	4	GND	-	-	-	Ground
	5	TYPEC1_SBU1	DP1_AUXP	-	-	Type-C 1 SBU1
	6	TYPEC1_SBU2	DP1_AUXN	-	-	Type-C 1 SBU2
	7	TYPEC0_USB20_VBUSDET	TYPEC1	-	-	Type-C 0 plug detection
	8	TYPEC0_SBU1	DP0_AUXP	-	-	Type-C 0 SBU1
	9	TYPEC0_SBU2	DP0_AUXN	-	-	Type-C 0 SBU1
	10	GND	-	-	-	Ground
	11	TYPEC0_OTG_D_N	-	-	-	Type-C 0 OTG data -
	12	TYPEC0_OTG_D_P	-	-	-	Type-C 0 OTG data +
	13	GND	-	-	-	Ground
	14	MIPI_DPHY1_RX_D0_P	MIPI_CPHY1_RX_TRIO0_B	-	-	MIPI DPHY 1 receiving data 0 +
	15	MIPI_DPHY1_RX_D0_N	MIPI_CPHY1_RX_TRIO0_A	-	-	MIPI DPHY 1 receiving data 0 -
	16	GND	-	-	-	Ground
	17	MIPI_DPHY1_RX_D1_P	MIPI_CPHY1_RX_TRIO1_A	-	-	MIPI DPHY 1 receiving data 1 +
	18	MIPI_DPHY1_RX_D1_N	MIPI_CPHY1_RX_TRIO0_C	-	-	MIPI DPHY 1 receiving data 1 -
	19	GND	-	-	-	Ground
	20	MIPI_DPHY1_RX_CLK_P	MIPI_CPHY1_RX_TRIO1_C	-	-	MIPI DPHY 1 receiving clock +
	21	MIPI_DPHY1_RX_CLK_N	MIPI_CPHY1_RX_TRIO1_B	-	-	MIPI DPHY 1 receiving clock -
	22	GND	-	-	-	Ground
	23	MIPI_DPHY1_RX_D2_P	MIPI_CPHY1_RX_TRIO2_B	-	-	MIPI DPHY 1 receiving data 2 +
	24	MIPI_DPHY1_RX_D2_N	MIPI_CPHY1_RX_TRIO2_A	-	-	MIPI DPHY 1 receiving data 2 -
	25	GND	-	-	-	Ground
	26	MIPI_DPHY1_RX_D3_P	-	-	-	MIPI DPHY 1 receiving data 3 +
	27	MIPI_DPHY1_RX_D3_N	MIPI_CPHY1_RX_TRIO2_C	-	-	MIPI DPHY 1 receiving data 3 -
	28	GND	-	-	-	Ground
	29	MIPI_DPHY0_RX_D0_P	MIPI_CPHY0_RX_TRIO0_B	-	-	MIPI DPHY 0 receiving data 0 +
	30	MIPI_DPHY0_RX_D0_N	MIPI_CPHY0_RX_TRIO0_A	-	-	MIPI DPHY 0 receiving data 0 -
	31	GND	-	-	-	Ground

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J1	32	MIPI_DPHY0_RX_D1_P	MIPI_CPHY0_RX_TRIO1_A	-	-	MIPI DPHY 0 receiving data 1 +
	33	MIPI_DPHY0_RX_D1_N	MIPI_CPHY0_RX_TRIO0_C	-	-	MIPI DPHY 0 receiving data 1 -
	34	GND	-	-	-	Ground
	35	MIPI_DPHY0_RX_CLK_P	MIPI_CPHY0_RX_TRIO1_C	-	-	MIPI DPHY 0 receiving clock +
	36	MIPI_DPHY0_RX_CLK_N	MIPI_CPHY0_RX_TRIO1_B	-	-	MIPI DPHY 0 receiving clock -
	37	GND	-	-	-	Ground
	38	MIPI_DPHY0_RX_D2_P	MIPI_CPHY0_RX_TRIO2_B	-	-	MIPI DPHY 0 receiving data 2 +
	39	MIPI_DPHY0_RX_D2_N	MIPI_CPHY0_RX_TRIO2_A	-	-	MIPI DPHY 0 receiving data 2 -
	40	GND	-	-	-	Ground
	41	MIPI_DPHY0_RX_D3_P	-	-	-	MIPI DPHY 0 receiving data 3 +
	42	MIPI_DPHY0_RX_D3_N	MIPI_CPHY0_RX_TRIO2_C	-	-	MIPI DPHY 0 receiving data 3 -
	43	GND	-	-	-	Ground
	44	PWRON_L	-	-	-	Power on
	45	PMIC_EXT_EN_OUT	-	-	-	External power control
	46	VCC4V0_SYS	-	-	-	4V power input
	47		-	-	-	4V power input
	48		-	-	-	4V power input
	49		-	-	-	4V power input
	50		-	-	-	4V power input

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J2	100	SDMMC_DET_L	GPIO	GPIO0_A4	1.8V	SD card plug detection
	99	WIFI_DISABLE1	GPIO	GPIO0_A0	1.8V	Wi-Fi antenna 1 disable
	98	SYS4V0_MODE_L	GPIO	GPIO0_C2	3.3V	Power mode selection
	97	WIFI_DISABLE2	CLK32K_IN /CLK32K_OUT0	GPIO0_B2	1.8V	Wi-Fi antenna 2 disable
	96	RTC_INT_L	SPI2_CS1_M2/I2C1_SCL_M1/ UART0_RX_M1	GPIO0_B0	1.8V	RTC interrupt
	95	SDMMC_PWREN	I2S1_LRCK_M1/PWM0_M0/ I2C2_SCL_M0/SPI0_CS1_M0/ PCIE30X1_1_PERSTN_M0	GPIO0_B7	3.3V	SD card enable
	94	PCIE_PWREN_H	CLK32K_OUT1	GPIO2_C5	1.8V	PCIe enable
	93	I2C4_SCL_M1	GMAC0_PPSTRING/FSPI_CS1N_ M1/HDMI_TX1_SCL_M0/ UART7_TX_M0	GPIO2_B5	1.8V	I^2C4 clock
	92	I2C4_SDA_M1	GMAC0_PTP_REFCLK/FSPI_CS0N _M1/HDMI_TX1_SDA_M0/ UART7_RX_M0	GPIO2_B4	1.8V	I^2C4 data
	91	TYPEC0_PWREN	I2S1_SDI0_M1/GPU_AVS/UART0_TX_ M0/ I2C4_SCL_M2/DP1_HPDIN_M1/ PWM4_M0/PCIE30X1_0_PERSTN_M0	GPIO0_C5	3.3V	Type-C 0 enable

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J2	90	TYPEC1_PWREN	ETH0_REFCLKO_25M/I2S2_SDI_ M0/I2C6_SCL_M2/SPI1_CS0_M0	GPIO2_C3	1.8V	Type-C 1 enable
	89	HDMI_RX_HPDIN_M1	PCIE30X2_PERSTN_M2/MCU_ JTAG_TCK_M1/UART9_RX_ M2/SPI0_CS0_M3	GPIO3_D4	3.3V	HDMI receiver hot plug detection
	88	GND	-	-	-	Ground
	87	GMAC1_TXD3	SDIO_D1_M1/ I2S3_SCLK/AUDDSM_LN/FSPI_ D1_M2/I2C6_SCL_M4/PWM11_ IR_ M0/ SPI4_MOSI_M1	GPIO3_A1	3.3V	RGMII/RMII 1 transmitting data 3
	86	GMAC1_TXD2	SDIO_D0_M1/I2S3_MCLK/FSPI_D0_ M2/I2C6_SDA_M4/PWM10_M0/ SPI4_MISO_M1	GPIO3_A0	3.3V	RGMII/RMII 1 transmitting data 2
	85	GMAC1_TXD1	I2S2_MCLK_M1/UART2_CTSN	GPIO3_B4	3.3V	RGMII/RMII 1 transmitting data 1
	84	GMAC1_TXD0	I2S2_SDO_M1/UART2_RTSN	GPIO3_B3	3.3V	RGMII/RMII 1 transmitting data 0
	83	GMAC1_TXEN	I2S2_SCLK_M1/UART3_TX_M1/ PWM12_M0	GPIO3_B5	3.3V	RGMII/RMII 1 transmitting control
	82	GMAC1_TXCLK	SDIO_CMD_M1/I2S3_SDI/ AUDDSM_RP/UART8_RTSN_M1/ SPI4_CS1_M1	GPIO3_A4	3.3V	RGMII/RMII 1 transmitting clock
	81	GND	-	-	-	Ground
	80	GMAC1_RXD3	SDIO_D3_M1/I2S3_SDO/AUDDSM_ RN/FSPI_D3_M2/UART8_RX_M1/ SPI4_CS0_M1	GPIO3_A3	3.3V	RGMII/RMII 1 receiving data 3
	79	GMAC1_RXD2	SDIO_D2_M1/I2S3_LRCK/AUDDSM_ LP/ FSPI_D2_M2/UART8_TX_M1/ SPI4_CLK_M1	GPIO3_A2	3.3V	RGMII/RMII 1 receiving data 2
	78	GMAC1_RXD1	MIPI_CAMERA3_CLK_M1/PWM9_M0	GPIO3_B0	3.3V	RGMII/RMII 1 receiving data 1
	77	GMAC1_RXD0	MIPI_CAMERA2_CLK_M1/PWM8_M0	GPIO3_A7	3.3V	RGMII/RMII 1 receiving data 0
	76	GMAC1_RXDV_CRS	MIPI_CAMERA4_CLK_M1/ UART2_TX_M2/PWM2_M1	GPIO3_B1	3.3V	RGMII/RMII 1 receiving control
	75	GMAC1_RXCLK	SDIO_CLK_M1/MIPI_CAMERA0_CLK_ M1/ FSPI_CLK_M2/I2C4_SDA_M0/ UART8_CTSN_M1	GPIO3_A5	3.3V	RGMII/RMII 1 receiving clock
	74	GND	-	-	-	Ground
	73	GMAC1_MDIO	MIPI_TE1/I2C8_SDA_M4/ UART7_CTSN_M1/PWM15_IR_M0/ SPI1_CS1_ M1	GPIO3_C3	3.3V	ENET management data input/output

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J2	72	GMAC1_MDC	MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1	GPIO3_C2	3.3V	ENET management data clock
	71	GMAC1_RSTnL	HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1	GPIO3_B7	3.3V	ENET reset
	70	TYPEC1_INT	GMAC1_MCLKINOUT/I2S2_LRCK_M1/UART3_RX_M1/PWM13_M0	GPIO3_B6	3.3V	Type-C 1 interrupt
	69	GND	-	-	-	Ground
	68	MIPI_CSI1_RX_D0_P	-	-	-	MIPI CSI 1 receiving data 0 +
	67	MIPI_CSI1_RX_D0_N	-	-	-	MIPI CSI 1 receiving data 0 -
	66	GND	-	-	-	Ground
	65	MIPI_CSI1_RX_D1_P	-	-	-	MIPI CSI 1 receiving data 1 +
	64	MIPI_CSI1_RX_D1_N	-	-	-	MIPI CSI 1 receiving data 1 -
	63	GND	-	-	-	Ground
	62	MIPI_CSI1_RX_CLK0_P	-	-	-	MIPI CSI 1 receiving clock 0 +
	61	MIPI_CSI1_RX_CLK0_N	-	-	-	MIPI CSI 1 receiving clock 0 -
	60	GND	-	-	-	Ground
	59	MIPI_CSI1_RX_D2_P	-	-	-	MIPI CSI 1 receiving data 2 +
	58	MIPI_CSI1_RX_D2_N	-	-	-	MIPI CSI 1 receiving data 2 -
	57	GND	-	-	-	Ground
	56	MIPI_CSI1_RX_D3_P	-	-	-	MIPI CSI 1 receiving data 3 +
	55	MIPI_CSI1_RX_D3_N	-	-	-	MIPI CSI 1 receiving data 3 -
	54	GND	-	-	-	Ground
	53	MIPI_CSI1_RX_CLK1_P	-	-	-	MIPI CSI 1 receiving clock 1 +
	52	MIPI_CSI1_RX_CLK1_N	-	-	-	MIPI CSI 1 receiving clock 1 -
	51	GND	-	-	-	Ground
	1	PWM3_M1_FAN	GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2	GPIO3_B2	3.3V	Fan PWM speed control
	2	5G_RESET	I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD	GPIO0_C6	3.3V	5G reset
	3	I2C6_SDA/M0	I2S1_SDI2_M1/PDM0_SDI0_M1/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_ WAKEN_M0	GPIO0_C7	3.3V	I^2C 6 data
	4	I2C6_SCL/M0	I2S1_SDI3_M1/PDM0_SDI1_M1/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0	GPIO0_D0	3.3V	I^2C 6 clock
	5	TYPEC0_INT	LITCPU_AVS/SPI3_CLK_M2	GPIO0_D3	3.3V	Type-C 0 interrupt
	6	TP1_INT_L	GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1	GPIO3_C0	3.3V	MIPI DSI 1 interrupt

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J2	7	TP2_RST_L	ETH1_REFCLKO_25M/MIPI_CAMERA1_CLK_M1/I2C4_SCL_M0	GPIO3_A6	3.3V	MIPI DSI 2 reset
	8	TP2_INT_L	PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/ PWM11_IR_M3/SPI0_CS1_M3	GPIO3_D5	3.3V	MIPI DSI 2 interrupt
	9	TP1_RST_L	GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1	GPIO3_C1	3.3V	MIPI DSI 1 reset
	10	I2C5_SCL_M0	CIF_D11/PCIE20X1_2_CLKREQN_M0/ HDMI_TX0_SCL_M2/ SPI3_MOSI_M3	GPIO3_C7	3.3V	I^2C 5 data
	11	I2C5_SDA_M0	CIF_D12/PCIE20X1_2_WAKEN_M0/ HDMI_ TX0_SDA_M2/UART4_RX_M1/ PWM8_M2/SPI3_CLK_M3	GPIO3_D0	3.3V	I^2C 5 clock
	12	GSENSOR_INT	GMAC0_PPSCLK/TEST_CLKOUT_M1/ HDMI_TX1_CEC_M0/UART9_RX_M0/ SPI1_CS1_M0	GPIO2_C4	1.8V	G-sensor interrupt
	13	GND	-	-	-	Ground
	14	GMAC0_TXD3	SDIO_CMD_M0/I2C3_SCL_M3	GPIO2_B2	1.8V	RGMII/RMII 0 transmitting data 3
	15	GMAC0_TXD2	SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0	GPIO2_B1	1.8V	RGMII/RMII 0 transmitting data 2
	16	GMAC0_TXD1	I2S2_SCLK_M0/I2C5_SDA_M4/ UART1_TX_M0	GPIO2_B7	1.8V	RGMII/RMII 0 transmitting data 1
	17	GMAC0_TXD0	I2S2_MCLK_M0/I2C5_SCL_M4/ UART1_RX_M0	GPIO2_B6	1.8V	RGMII/RMII 0 transmitting data 0
	18	GMAC0_TXEN	I2S2_LRCK_M0/I2C2_SDA_M1/ UART1_RTSN_M0/SPI1_CLK_M0	GPIO2_C0	1.8V	RGMII/RMII 0 transmitting control
	19	GMAC0_TXCLK	SDIO_CLK_M0/FSPI_CLK_M1/ I2C3_SDA_M3	GPIO2_B3	1.8V	RGMII/RMII 0 transmitting clock
	20	GND	-	-	-	Ground
	21	GMAC0_RXD3	SDIO_D1_M0/FSPI_D1_M1/ UART6_TX_M0	GPIO2_A7	1.8V	RGMII/RMII 0 receiving data 3
	22	GMAC0_RXD2	SDIO_D0_M0/FSPI_D0_M1/ UART6_RX_M0	GPIO2_A6	1.8V	RGMII/RMII 0 receiving data 2
	23	GMAC0_RXD1	I2C6_SDA_M2/UART9_TX_M0/ SPI1_MOSI_M0	GPIO2_C2	1.8V	RGMII/RMII 0 receiving data 1
	24	GMAC0_RXD0	I2C2_SCL_M1/UART1_CTSN_M0/ SPI1_MISO_M0	GPIO2_C1	1.8V	RGMII/RMII 0 receiving data 0
	25	GMAC0_RXDV_CRS	UART7_RTSN_M0/PWM2_M2/ SPI3_CS0_M0	GPIO4_C2	1.8V	RGMII/RMII 0 receiving control
	26	GMAC0_RXCLK	SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0	GPIO2_B0	1.8V	RGMII/RMII 0 receiving clock

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J2	28	GMAC0_MDIO	I2C0_SCL_M1/UART9_CTSN_M0/ PWM6_M2/SPI3_MOSI_M0	GPIO4_C5	1.8V	ENET management data input/output
	29	GMAC0_MDC	I2C7_SDA_M1/UART9_RTSN_M0/ PWM5_M2/SPI3_MISO_M0	GPIO4_C4	1.8V	ENET management data clock
	30	GMAC0_RSTn_L	2C0_SDA_M1/UART7_CTSN_M0/ PWM7_IR_M3/SPI3_CLK_M0	GPIO4_C6	1.8V	ENET reset
	31	PHONE_CTL	GMAC0_MCLKINOUT/I2S2_SDO_ M0/I2C7_SCL_M1/PWM4_M1/ SPI3_CS1_M0	GPIO4_C3	1.8V	Earphone control
	32	GND	-	-	-	Ground
	33	MIPI_CSI0_RX_D0_N	-	-	-	MIPI CSI 0 receiving data 0 -
	34	MIPI_CSI0_RX_D0_P	-	-	-	MIPI CSI 0 receiving data 0 +
	35	GND	-	-	-	Ground
	36	MIPI_CSI0_RX_D1_N	-	-	-	MIPI CSI 0 receiving data 1 -
	37	MIPI_CSI0_RX_D1_P	-	-	-	MIPI CSI 0 receiving data 1 +
	38	GND	-	-	-	Ground
	39	MIPI_CSI0_RX_CLK0_N	-	-	-	MIPI CSI 0 receiving clock 0 -
	40	MIPI_CSI0_RX_CLK0_P	-	-	-	MIPI CSI 0 receiving clock 0 +
	41	GND	-	-	-	Ground
	42	MIPI_CSI0_RX_D2_N	-	-	-	MIPI CSI 0 receiving data 2 -
	43	MIPI_CSI0_RX_D2_P	-	-	-	MIPI CSI 0 receiving data 2 +
	44	GND	-	-	-	Ground
	45	MIPI_CSI0_RX_D3_N	-	-	-	MIPI CSI 0 receiving data 3 -
	46	MIPI_CSI0_RX_D3_P	-	-	-	MIPI CSI 0 receiving data 3 +
	47	GND	-	-	-	Ground
	48	MIPI_CSI0_RX_CLK1_N	-	-	-	MIPI CSI 0 receiving clock 1 -
	49	MIPI_CSI0_RX_CLK1_P	-	-	-	MIPI CSI 0 receiving clock 1 +
	50	GND	-	-	-	Ground

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J3	100	GND	-	-	-	Ground
	99	SDMMC0_D0	PDM1_SDI3_M0/JTAG_TCK_M1/ I2C3_SCL_M4/UART2_TX_M1/ PWM8_M1	GPIO4_D0	3.3V	SDMMC 0 data 0
	98	SDMMC0_D1	PDM1_SDI2_M0/JTAG_TMS_M1/ I2C3_SDA_M4/UART2_RX_M1/ PWM9_M1	GPIO4_D1	3.3V	SDMMC 0 data 1
	97	SDMMC0_D2	PDM1_SDI1_M0/JTAG_TCK_M0/ I2C8_SCL_M0/UART5_CTSN_M0	GPIO4_D2	3.3V	SDMMC 0 data 2

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J3	96	SDMMC0_D3	PDM1_SDI0_M0/JTAG_TMS_M0/ I2C8_SDA_M0/UART5_RTSN_M0/ PWM10_M1	GPIO4_D3	3.3V	SDMMC 0 data 3
	95	SDMMC0_CMD	PDM1_CLK1_M0/MCU_JTAG_TCK_M0/ UART5_RX_M0/PWM7_IR_M1	GPIO4_D4	3.3V	SDMMC 0 command
	94	SD_CLK	PDM1_CLK0_M0/TEST_CLKOUT_M0/ MCU_JTAG_TMS_M0/UART5_TX_M0	GPIO4_D5	3.3V	SDMMC clock
	93	GND	-	-	-	Ground
	92	HDMI0_TX_SBD_N	eDP0_TX_AUX_N	-	-	HDMI 0 transmitter sideband -
	91	HDMI0_TX_SBD_P	eDP0_TX_AUX_P	-	-	HDMI 0 transmitter sideband +
	90	GND	-	-	-	Ground
	89	HDMI0_TX3_N	eDP0_TX_D3_N	-	-	HDMI 0 transmitter 3 -
	88	HDMI0_TX3_P	eDP0_TX_D3_P	-	-	HDMI 0 transmitter 3 +
	87	GND	-	-	-	Ground
	86	HDMI0_TX0_N	eDP0_TX_D0_N	-	-	HDMI 0 transmitter 0 -
	85	HDMI0_TX0_P	eDP0_TX_D0_P	-	-	HDMI 0 transmitter 0 +
	84	GND	-	-	-	Ground
	83	HDMI0_TX1_N	eDP0_TX_D1_N	-	-	HDMI 0 transmitter 1 -
	82	HDMI0_TX1_P	eDP0_TX_D1_P	-	-	HDMI 0 transmitter 1 +
	81	GND	-	-	-	Ground
	80	HDMI0_TX2_N	eDP0_TX_D2_N	-	-	HDMI 0 transmitter 2 -
	79	HDMI0_TX2_P	eDP0_TX_D2_P	-	-	HDMI 0 transmitter 2 +
	78	GND	-	-	-	Ground
	77	HDMI1_TX_SBD_N	eDP1_TX_AUX_N	-	-	HDMI 1 transmitter sideband -
	76	HDMI1_TX_SBD_P	eDP1_TX_AUX_P	-	-	HDMI 1 transmitter sideband +
	75	GND	-	-	-	Ground
	74	HDMI1_TX3_N	eDP1_TX_D3_N	-	-	HDMI 1 transmitter 3 -
	73	HDMI1_TX3_P	eDP1_TX_D3_P	-	-	HDMI 1 transmitter 3 +
	72	GND	-	-	-	Ground
	71	HDMI1_TX0_N	eDP1_TX_D0_N	-	-	HDMI 1 transmitter 0 -
	70	HDMI1_TX0_P	eDP1_TX_D0_P	-	-	HDMI 1 transmitter 0 +
	69	GND	-	-	-	Ground
	68	HDMI1_TX1_N	eDP1_TX_D1_N	-	-	HDMI 1 transmitter 1 -
	67	HDMI1_TX1_P	eDP1_TX_D1_P	-	-	HDMI 1 transmitter 1 +
	66	GND	-	-	-	Ground
	65	HDMI1_TX2_N	eDP1_TX_D2_N	-	-	HDMI 1 transmitter 2 -
	64	HDMI1_TX2_P	eDP1_TX_D2_P	-	-	HDMI 1 transmitter 2 +
	63	GND	-	-	-	Ground
	62	HDMI_RX_CLK_N	-	-	-	HDMI receiver clock -
	61	HDMI_RX_CLK_P	-	-	-	HDMI receiver clock +

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J3	60	GND	-	-	-	Ground
	59	HDMI_RX_D0_N	-	-	-	HDMI receiving data 0 -
	58	HDMI_RX_D0_P	-	-	-	HDMI receiving data 0 +
	57	GND	-	-	-	Ground
	56	HDMI_RX_D1_N	-	-	-	HDMI receiving data 1 -
	55	HDMI_RX_D1_P	-	-	-	HDMI receiving data 1 +
	54	GND	-	-	-	Ground
	53	HDMI_RX_D2_N	-	-	-	HDMI receiving data 2 -
	52	HDMI_RX_D2_P	-	-	-	HDMI receiving data 2 +
	51	GND	-	-	-	Ground
	1	GND	-	-	-	Ground
	2	BOOT_SARADC_IN0	-	-	-	Flashing mode determination based on the button status
	3	SARADC_VIN1	-	-	-	SARADC_VIN1_KEY/RECOVERY
	4	SARADC_VIN2	-	-	-	SARADC_VIN2
	5	SARADC_VIN3	-	-	-	SARADC_VIN3_HP_HOOK
	6	SARADC_VIN4	-	-	-	SARADC_VIN4
	7	SARADC_VIN5	-	-	-	SARADC_VIN5_HW_ID
	8	SARADC_VIN6	-	-	-	SARADC_VIN6
	9	SARADC_VIN7	-	-	-	SARADC_VIN7_LCD_ID0
	10	HDMITX1_SDA_M1	CIF_D9/FSPI_CS1N_M2/PCIE30 X4_WAKEN_M2/UART5_RX_M1 /SPI3_CS1_M3	GPIO3_C5	3.3V	HDMI 1 transmitter I^2C data
	11	HDMITX1_SCL_M1	CIF_D10/PCIE30X4_ PERSTN _M2/SPI3_MISO_M3	GPIO3_C6	3.3V	HDMI 1 transmitter I^2C clock
	12	HDMITX1_CEC_M2	CIF_D8/FSPI_CS0N_M2/PCIE30 X4_CLKREQN_M2/UART5_TX_M1/ SPI3_CS0_M3	GPIO3_C4	3.3V	HDMI 1 transmitter CEC
	13	HDMI_RX_SCL_M1	CIF_D14/PCIE30X2_CLKREQN_ M2/I2C7_SCL_M2/UART9_RTSN_ M2/ SPI0_MOSI_M3	GPIO3_D2	3.3V	HDMI receiver I^2C clock
	14	HDMI_RX_SDA_M1	CIF_D15/PCIE30X2_WAKEN_M2/ I2C7_SDA_M2/UART9_CTSN_M2/ PWM10_M2/SPI0_CLK_M3	GPIO3_D3	3.3V	HDMI receiver I^2C data
	15	HDMI_RX_CEC_M1	CIF_D13/PCIE20X1_2_PERSTN_M0/ UART4_TX_M1/PWM9_M2/ SPI0_MISO_M3	GPIO3_D1	3.3V	HDMI receiver CEC
	16	HDMITX0_SDA_M0	BT1120_D14/PCIE20X1_2_WAKEN_ M1/ I2C8_SCL_M3/SPI3_CS0_M1	GPIO4_C0	3.3V	HDMI 0 transmitter I^2C data

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J3	17	HDMITX0_SCL_M0	BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/ SPI3_CLK_M1	GPIO4_B7	3.3V	HDMI 0 transmitter I^2C clock
	18	HDMITX0_CEC_M0	BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/I2C8_SDA_M3/PWM6_M1/ SPI3_CS1_M1	GPIO4_C1	3.3V	HDMI 0 transmitter CEC
	19	HDMI0_TX_ON_H	MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1	GPIO4_B1	3.3V	HDMI 0 transmitter output enable
	20	TYPEC0_USB20_OTG_ID	-	-	-	TYPEC0_USB20_OTG_ID
	21	TYPEC1_USB20_OTG_ID	-	-	-	TYPEC1_USB20_OTG_ID
	22	CAN1_TX_M1	CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1	GPIO4_B3	3.3V	CAN 1 transmitter
	23	CAN1_RX_M1	CIF_HREF/BT1120_D8/I2S1_ SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/ SPI0_CS0_M1	GPIO4_B2	3.3V	CAN 1 receiver
	24	SPK_CTL_H	CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1	GPIO4_B0	3.3V	Speaker control
	25	TYPEC0_SBU2_DC	UART9_CTSN_M1/SPI0_MOSI_M1	GPIO4_A1	3.3V	Type-C 0 SBU2
	26	TYPEC0_SBU1_DC	CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1	GPIO4_A0	3.3V	Type-C 0 SBU1
	27	UART3_TX_M2	CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/SPI2_MOSI_M1	GPIO4_A5	3.3V	UART 3 transmitting data
	28	UART3_RX_M2	CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1	GPIO4_A6	3.3V	UART 3 receiving data
	29	TYPEC1_SBU2_DC	CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1	GPIO4_A7	3.3V	Type-C 1 SBU2

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J3	30	TYPEC1_SBU1_DC	CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1	GPIO4_A2	3.3V	Type-C 1 SBU1
	31	TYPEC1_USB20_VBUSDET	-	-	-	VBUS power detection
	32	GND	-	-	-	Ground
	33	TYPEC1_SSRX1_N	DP1_TX0N	-	-	Type-C 1 receiver 1 -
	34	TYPEC1_SSRX1_P	DP1_TX0P	-	-	Type-C 1 receiver 1 +
	35	GND		-	-	Ground
	36	TYPEC1_SSTX1_N	DP1_TX1N	-	-	Type-C 1 transmitter 1 -
	37	TYPEC1_SSTX1_P	DP1_TX1P	-	-	Type-C 1 transmitter 1 +
	38	GND		-	-	Ground
	39	TYPEC1_SSRX2_N	DP1_TX2N	-	-	Type-C 1 receiver 2 -
	40	TYPEC1_SSRX2_P	DP1_TX2P	-	-	Type-C 1 receiver 2 +
	41	GND		-	-	Ground
	42	TYPEC1_SSTX2_N	DP1_TX3N	-	-	Type-C 1 transmitter 2 -
	43	TYPEC1_SSTX2_P	DP1_TX3P	-	-	Type-C 1 transmitter 2 +
	44	GND	-	-	-	Ground
	45	USB20_HOST0_D_P	-	-	-	USB 2.0 Host 0 data +
	46	USB20_HOST0_D_N	-	-	-	USB 2.0 Host 0 data -
	47	GND	-	-	-	Ground
	48	USB20_HOST1_D_P	-	-	-	USB 2.0 Host 1 data +
	49	USB20_HOST1_D_N	-	-	-	USB 2.0 Host 1 data -
	50	GND	-	-	-	Ground

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J4	100	I2C2_SDA_M4	CIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/UART6_RX_M1/SPI4_MISO_M2	GPIO1_A0	1.8V	I^2C2 data
	99	I2C2_SCL_M4	PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/UART6_TX_M1/SPI4_MOSI_M2	GPIO1_A1	1.8V	I^2C2 clock
	98	MIPI_CAM3_PDN_L	PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0	GPIO1_A7	1.8V	MIPI CSI 3 power down control
	97	MIPI_CAM3_RST_L	DM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2	GPIO1_B1	1.8V	MIPI CSI 3 reset
	96	MIPI_CAM4_PDN_L	PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0	GPIO1_B0	1.8V	MIPI CSI 4 power down control

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J4	95	MIPI_CAM4_RST_L	PDM1_SDI3_M1/PCIE30X4_ PERSTN_M3/UART4_RX_M2/ SPI0_MOSI_M2	GPIO1_B2	1.8V	MIPI CSI 4 reset
	94	MIPI_CAM3_CLKOUT	HDMI_RX_SCL_M2/I2C8_SCL_M2 / UART1_RTSN_M1/PWM14_M2	GPIO1_D6	1.8V	MIPI CSI 3 clock output
	93	MIPI_CAM4_CLKOUT	PCIE30X2_CLKREQN_M3/HDMI_ RX_SDA_M2/I2C8_SDA_M2/UART 1_CTSN_M1/PWM15_IR_M3	GPIO1_D7	1.8V	MIPI CSI 4 clock output
	92	I2C3_SDA_M0	UART3_RX_M0/SPI4_MISO_M0	GPIO1_C0	1.8V	I^2C 3 data
	91	I2C3_SCL_M0	UART3_TX_M0/SPI4_MOSI_M0	GPIO1_C1	1.8V	I^2C 3 clock
	90	LCD_BL2_PWM15	PDM0_CLK0_M0/I2C4_SDA_M4	GPIO1_C6	1.8V	MIPI DSI 2 backlight control
	89	HDMIRX_DET_L	PDM0_SDI0_M0/SPI1_CS1_M2	GPIO1_D5	1.8V	HDMI receiver detection
	88	HDMI1_TX_ON_H	PDM0_CLK1_M0/I2C2_SDA_M3 /PWM11_IR_M2/SPI4_CS1_M0	GPIO1_C4	1.8V	HDMI 1 transmitter output enable
	87	HDMIRX_HPDOUT_H	I2S0_SDI0	GPIO1_D4	1.8V	HDMI receiver hot plug detection control
	86	MIPI_CAM1_RST_L	2S0_SDO3/I2S0_SDI2/PDM0_SD I2_M0/I2C1_SCL_M4/UART4_TX _M0/PWM0_M1/SPI1_CLK_M2	GPIO1_D2	1.8V	MIPI CSI 1 reset
	85	HDMITX0_HPDIN_M0	SPI2_MOSI_M0	GPIO1_A5	1.8V	HDMI 0 transmitter hot plug detection
	84	PCIE30X4_WAKEn_M1_L	BT1120_D11/HDMI_RX_CEC_M0 /SATA1_ACT_LED_M0/UART9_ RX_M1/PWM12_M1/ SPI3_MISO_M1	GPIO4_B5	3.3V	PCIe 3.0 x4 wake up
	83	PCIE30X4_CLKREQn_M1_L	CIF_CLKOUT/BT1120_D10/I2S1_ SDO3_M0/DP0_HPDIN_M0/ SPDIF0_TX_M1/UART9_TX_M1/ PWM11_IR_M1	GPIO4_B4	3.3V	PCIe 3.0 x4 clock request
	82	PCIE30X4_PERSTn_M1_L	BT1120_D12/HDMI_RX_HPD IN_M0/SATA0_ACT_LED_M0/ I2C5_SCL_M1/ PWM13_M1/SPI3_MOSI_M1	GPIO4_B6	3.3V	PCIe 3.0 x4 reset
	81	GND	-	-	-	Ground
	80	PCIE30_PORT1_REFCLK_IN_P	-	-	-	PCIe 3.0_1 reference clock +
	79	PCIE30_PORT1_REFCLK_IN_N	-	-	-	PCIe 3.0_1 reference clock -
	78	GND	-	-	-	Ground
	77	PCIE30_PORT1_TX3_N	-	-	-	PCIe 3.0_1 transmitter 3 -
	76	PCIE30_PORT1_TX3_P	-	-	-	PCIe 3.0_1 transmitter 3 +
	75	GND	-	-	-	Ground

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J4	74	PCIE30_PORT1_TX2_N	-	-	-	PCIe 3.0_1 transmitter 2 -
	73	PCIE30_PORT1_TX2_P	-	-	-	PCIe 3.0_1 transmitter 2 +
	72	GND	-	-	-	Ground
	71	PCIE30_PORT1_RX3_N	-	-	-	PCIe 3.0_1 receiver 3 -
	70	PCIE30_PORT1_RX3_P	-	-	-	PCIe 3.0_1 receiver 3 +
	69	GND	-	-	-	Ground
	68	PCIE30_PORT1_RX2_N	-	-	-	PCIe 3.0_1 receiver 2 -
	67	PCIE30_PORT1_RX2_P	-	-	-	PCIe 3.0_1 receiver 2 +
	66	GND	-	-	-	Ground
	65	USB30_2_SSTX_P	-	-	-	USB 3.0_2 transmitter +
	64	USB30_2_SSTX_N	-	-	-	USB 3.0_ 2 transmitter -
	63	GND	-	-	-	Ground
	62	USB30_2_SSRX_P	-	-	-	USB 3.0_2 receiver +
	61	USB30_2_SSRX_N	-	-	-	USB 3.0_2 receiver -
	60	GND	-	-	-	Ground
	59	PCIE20_0_REFCLK_P	-	-	-	PCIe 2.0_0 reference clock +
	58	PCIE20_0_REFCLK_N	-	-	-	PCIe 2.0_0 reference clock -
	57	GND	-	-	-	Ground
	56	SATA30_0_TX_P	-	-	-	SATA 3.0_0 transmitter +
	55	SATA30_0_TX_N	-	-	-	SATA 3.0_0 transmitter -
	54	GND	-	-	-	Ground
	53	SATA30_0_RX_P	-	-	-	SATA 3.0_0 receiver +
	52	SATA30_0_RX_N	-	-	-	SATA 3.0_0 receiver -
	51	GND	-	-	-	Ground
	1	MIPI_CAM1_PDN_L	VOP_POST_EMPTY/I2C4_SDA_ M3/UART6_RTSN_M1/PWM0_M2/ SPI4_CLK_M2	GPIO1_A2	1.8V	MIPI CSI 1 power down control
	2	MIPI_CAM1_CLKOUT	SPDIF0_TX_M0/PCIE30X2_ WAKEN_M3/HDMI_RX_HPDIN_ M2/I2C5_SCL_M3/UART1_TX_M1	GPIO1_B6	1.8V	MIPI CSI 1 clock output
	3	HDMITX1_HPDIN_M0	SPI2_CLK_M0	GPIO1_A6	1.8V	HDMI 1 transmitter hot plug detection
	4	MIPI_CAM2_PDN_L	HDMI_TX1_SCL_M2/ SPI2_MISO_M0	GPIO1_A4	1.8V	MIPI CSI 2 power down control
	5	MIPI_CAM2_CLKOUT	SPDIF1_TX_M0/PCIE30X2_PE RSTN_M3/HDMI_RX_CEC_M2/ SATA2_ACT_LED_M1/I2C5_SDA_ M3/UART1_RX_M1/PWM13_M2	GPIO1_B7	1.8V	MIPI CSI 2 clock output

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J4	6	MIPI_CAM2_RST_L	I2S0_SDI1/PDM0_SDI3_M0/ I2C1_SDA_M4/UART4_RX_M0/ PWM1_M1/SPI1_CS0_M2	GPIO1_D3	1.8V	MIPI CSI 2 reset
	7	WORKING_LEDEN_H	HDMI_TX1_SDA_M2/I2C4_SCL_ M3/UART6_CTSN_M1/ PWM1_M2/SPI4_CS0_M2	GPIO1_A3	1.8V	Carrier board working indicator
	8	LCD_BL1_PWM1	PDM0_CLK0_M1/ I2C2_SDA_M0/ SPI0_MOSI_M0/PCIE30X1_0 _CLKREQN_M0	GPIO0_C0	3.3V	MIPI DSI 1 backlight control
	9	UART2_RX_M0	I2S1_SCLK_M1/JTAG_TMS_M2/I2C1 _SDA_M0/PCIE30X1_1_WAKEN_M0	GPIO0_B6	3.3V	UART 2 receiving data
	10	UART2_TX_M0	I2S1_MCLK_M1/JTAG_TCK_M2/I2C1 _SCL_M0/PCIE30X1_1_CLKREQN_M0	GPIO0_B5	3.3V	UART 2 transmitting data
	11	GPIO	PDM0_CLK1_M1/PWM2_M0/UART 0_RX_M0/I2C4_SDA_M2/ DP0_HPD IN_M1/PCIE30X1_0_WAKEN_M0	GPIO0_C4	3.3V	No connection
	12	I2S0_SDI0	-	GPIO1_D4	1.8V	I^2S 0 data input
	13	I2S0_LRCK_TX	I2C2_SCL_M3/UART4_RTSN	GPIO1_C5	1.8V	I^2S 0 left-right channel clock
	14	I2S0_SDO0	I2C4_SCL_M4/UART4_CTSN	GPIO1_C7	1.8V	I^2S 0 data output
	15	I2S0_SCLK_TX	2C6_SCL_M1/UART3_CTSN/PWM7_ IR_M2/SPI4_CS0_M0	GPIO1_C3	1.8V	I^2S 0 clock
	16	I2S0_MCLK	I2C6_SDA_M1/UART3_RTSN/ PWM3_IR_M2/SPI4_CLK_M0	GPIO1_C2	1.8V	I^2S 0 master clock
	17	I2C7_SCL_M0/CODEC	I2C7_SCL_M0/UART6_TX_M2/ SPI1_MISO_M2	GPIO1_D0	1.8V	I^2C7 clock
	18	I2C7_SDA_M0/CODEC	I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA _M0/UART6_RX_M2/SPI1_MOSI_M2	GPIO1_D1	1.8V	I^2C7 data
	19	HP_DET_L	PDM0_CLK1_M0/I2C2_SDA_M3/ PWM11_IR_M2/SPI4_CS1_M0	GPIO1_C4	1.8V	Headphone plug detection
	20	PCIEx1_0_PERSTn_M1_L	PDM1_CLK0_M1/PCIE30X1_0_PERSTN _M2/UART7_RX_M2/SPI0_CS0_M2	GPIO1_B4	1.8V	PCIe 3.0 x1 reset
	21	PCIE30x1_0_CLKREQn_M1_L	UART7_TX_M2/SPI0_CS1_M2	GPIO1_B5	1.8V	PCIe 3.0 x1 clock request
	22	PCIE30x1_0_WAKEn_M1_L	PDM1_CLK1_M1/PCIE30X1_0_WAKEN _M2/SATA0_ACT_LED_M1/UART4_ TX_M2/SPI0_CLK_M2	GPIO1_B3	1.8V	PCIe 3.0 x1 wakeup
	23	GND	-	-	-	Ground
	24	PCIE30_PORT0_TX1_N	-	-	-	PCIe 3.0_0 transmitter 1 -
	25	PCIE30_PORT0_TX1_P	-	-	-	PCIe 3.0_0 transmitter 1 +

Header	Pin	Function 1	Function 2	GPIO	Level	Description
J4	26	GND	-	-	-	Ground
	27	PCIE30_PORT0_TX0_N	-	-	-	PCIe 3.0_0 transmitter 0 -
	28	PCIE30_PORT0_TX0_P	-	-	-	PCIe 3.0_0 transmitter 0 +
	29	GND	-	-	-	Ground
	30	PCIE30_PORT0_REFCLK_IN_N	-	-	-	PCIe 3.0_0 reference clock -
	31	PCIE30_PORT0_REFCLK_IN_P	-	-	-	PCIe 3.0_0 reference clock +
	32	GND	-	-	-	Ground
	33	PCIE30_PORT0_RX1_N	-	-	-	PCIe 3.0_0 receiver 1 clock -
	34	PCIE30_PORT0_RX1_P	-	-	-	PCIe 3.0_0 receiver 1 clock +
	35	GND	-	-	-	Ground
	36	PCIE30_PORT0_RX0_N	-	-	-	PCIe 3.0_0 receiver 0 clock -
	37	PCIE30_PORT0_RX0_P	-	-	-	PCIe 3.0_0 receiver 0 clock +
	38	GND	-	-	-	Ground
	39	PCIE20_2_REFCLK_N	-	-	-	PCIe 2.0_2 reference clock -
	40	PCIE20_2_REFCLK_P	-	-	-	PCIe 2.0_2 reference clock +
	41	GND	-	-	-	Ground
	42	PCIE20_1_REFCLK_N	-	-	-	PCIe 2.0_1 reference clock -
	43	PCIE20_1_REFCLK_P	-	-	-	PCIe 2.0_1 reference clock +
	44	GND	-	-	-	Ground
	45	PCIE20_1_TX_P	SATA30_1_TX_P	-	-	PCIe 2.0_1 transmitter +
	46	PCIE20_1_TX_N	SATA30_1_TX_N	-	-	PCIe 2.0_1 transmitter -
	47	GND		-	-	Ground
	48	PCIE20_1_RX_P	SATA30_1_RX_P	-	-	PCIe 2.0_1 receiver +
	49	PCIE20_1_RX_N	SATA30_1_RX_N	-	-	PCIe 2.0_1 receiver -
	50	GND	-	-	-	Ground

Since its establishment in 2002 by two Silicon Valley entrepreneurs, Vantron Technology has been at the forefront of the connected IoT devices and IoT platform solutions. Today, Vantron boasts a global customer base that includes many Fortune Global 500 companies. Its product lines cover edge intelligent hardware, IoT communication devices, industrial displays and BlueSphere cloud platforms.

With over 20 years of experience in R&D of intelligent edge hardware, Vantron has provided users with diverse embedded solutions featuring ARM and X86 architectures. Its offerings range from Linux, Android to Windows, from embedded to desktop level, and from gateways to servers. In addition, it provides users with system trimming, driver transplantation and more to cater to the unique needs of its users.