VOSM800 System-on-Module



Product Brief

The VOSM800 system-on-module is powered by NXP i.MX 8M Mini processor with maximum clock frequency up to 1.8GHz. The module integrates a quad-core Arm Cortex-A53 processor and provides up to 4GB LPDDR4 memory and 64GB eMMC storage. Equipped with dedicated hardware video processing engines, it supports H.264 encoding and H.264/H.265 decoding at resolutions up to 1080p@60 fps for low-latency multimedia applications.

The module features a variety of expansion interfaces, including video output interfaces, on-board Wi-Fi and Bluetooth, USB 2.0, and GPIOs to increase its versatility for diverse scenarios. The module features an LGA packaging that allows for direct soldering, eliminating the need for additional connectors. Additionally, it is compliant with Open Standard Modules (OSM) V1.1, which enables seamless integration into various products. Moreover, the module provides a long product lifecycle that meets the rigorous demands of industrial customers.

The module is designed to cater to a vast of application scenarios including but not limited to handheld devices, smart home appliances, industrial IoT devices, and gym instruments.

Features and benefits

VOSM800
Flexible option for advanced & compact editions
Rich interfaces, robust system performance
1080p@60fps H.264 encoder & H.265 decoder
On-board Wi-Fi & Bluetooth
Android OS, Linux support upon request
Compact size, LGA packaging
Open Standard Modules (OSM) V1.1 compliant
Extended service life (7+ years)

Application Scenarios


Robotics


Security & Surveillance


Fitness Console



Home Appliance


Industrial IoT



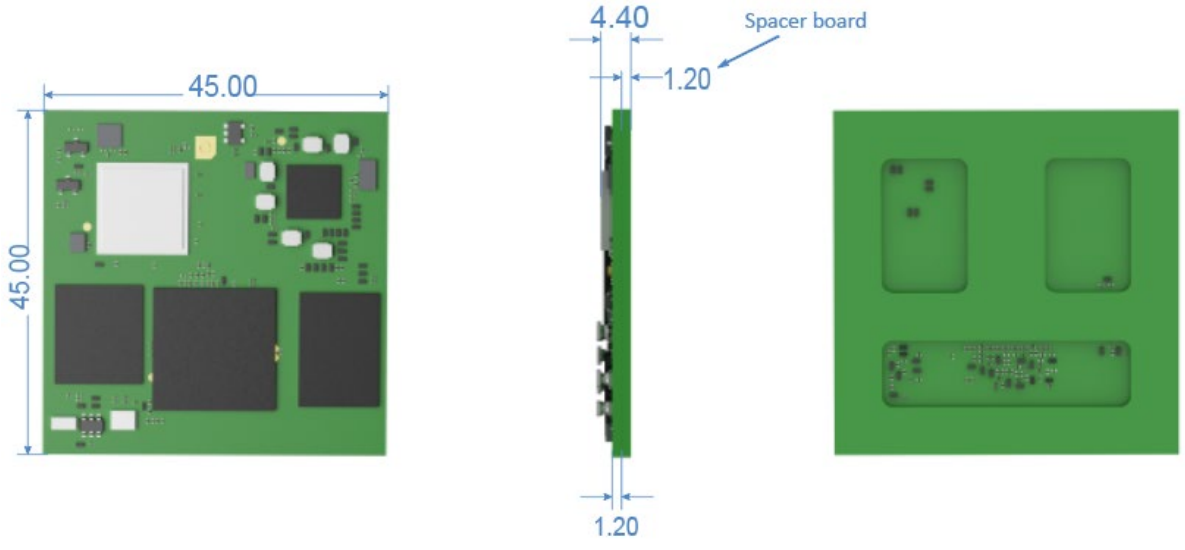
Smart Retail

VOSM800 System-on-Module Datasheet

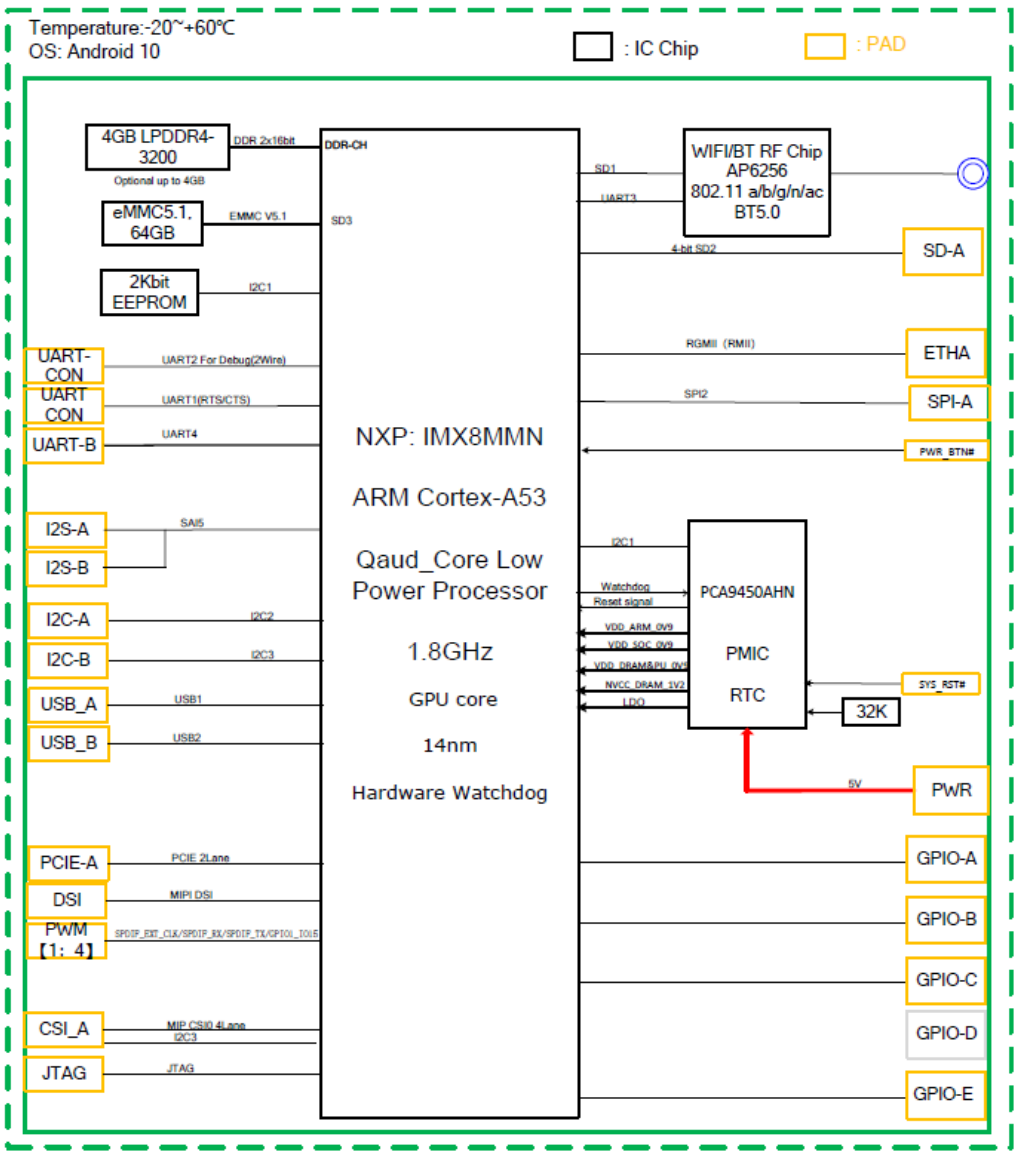
Specifications			
System	CPU	NXP i.MX 8M Mini, Quad-core ARM Cortex-A53, up to 1.8GHz	
	Memory	2GB LPDDR4 (Optional: 4GB)	
	Storage	16GB eMMC 5.1 (Optional: 64GB)	
	EEPROM	2Kb (for hardware configuration information)	
Communication	Wi-Fi	Wi-Fi 802.11 a/b/g/n/ac	
	Bluetooth	Bluetooth 5.0	
Media	Video processing	1080p60 H265, VP9 decoder 1080p60 H264, VP8 decoder	1080p60 H.264, VP8 encoder
	Graphics processing	GCNanoUltra for 3D acceleration	GC320 for 2D acceleration
Power	Input	5V/2A DC input	
Software	Operating system	Android 11, Linux (Support upon request)	
	Device management	BlueSphere MDM (Optional for Android version)	
Mechanical	Dimensions	45mm × 45mm × 4.4mm	
Environmental Condition	Temperature	Operating: -20℃ ~ +60℃ (Optional: -40℃ ~ +85℃)	Storage: -20℃ ~ +70℃
	Humidity	≤95% RH (Non-condensing)	
	Certification	CE, FCC	

I/O		
MIPI DSI	1 × 4-lane MIPI DSI, up to 1080P @60Hz	
MIPI CSI	1 × 4-lane MIPI CSI	
I^2S	1 × I^2S	
SDIO	1 × 4-bit SDIO V3.0	
RGMII (Ethernet)	1 × RGMII	
SPI	1 × SPI	
UART	1 × Debug UART (1.8V level)	2 × Communication UART
USB	1 × USB 2.0 Host	1 × USB 2.0 OTG
PCIe	1 × PCIe 2.0	
I^2C	2 × I^2C	
GPIO	25 × GPIO	
JTAG	Supported	
Key Signal	1 × Power key	1 × Reset key
PWM	2 × PWM	

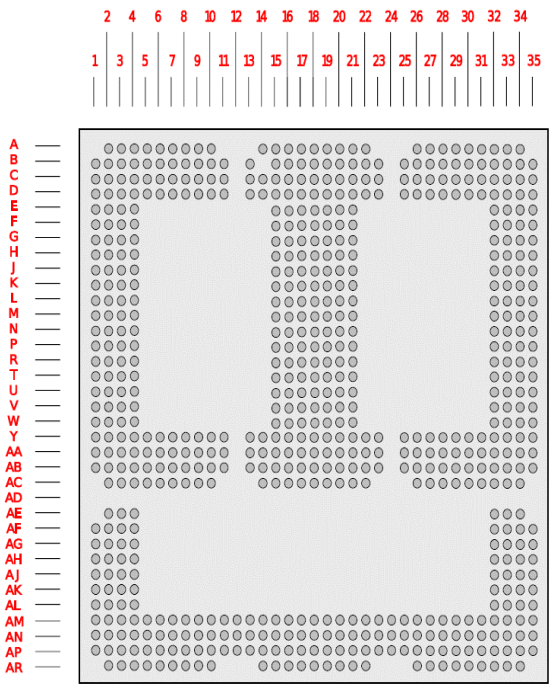
Mechanical Outline



Block Diagram



Pinout



(View from top, through the module)

In the sheets below:

* **Pin** refers to the pin number defined by OSM as shown in above figure.

* **Signal** refers to the pin name used by Vantron.

* **CPU Ball #** refers to the corresponding designations of the i.MX 8M Mini CPU.

* Certain signals are derived from auxiliary ICs and the corresponding IC names are provided accordingly.

* Unless otherwise explicitly stated, all I/O signals use a **1.8V level**.

Pin*	Signal*	CPU Ball #*	Description
U19, R18	NC		No connection
V17	EXT_EN	AF16	Module control / GPIO
T17	BOOT_MODE1	G27	The module enters recovery mode if low on carrier board.
AA9	PWRKEY	A25	Power button input from carrier board. Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the module.
W17	NC		No connection
U17	nRST	PMIC_8	Reset input from carrier board, active low
AB18, AA18	NC		No connection
M19, Y16, Y20	NC		No connection
Y3, C5, AA33	NC		No connection
Y25	VCC_IN_5V		**5V** power input for the module
Y26	VCC_IN_5V		**5V** power input for the module
Y27	VCC_IN_5V		**5V** power input for the module
Y28	VCC_IN_5V		**5V** power input for the module
D18, E15, E21	GND		Ground
F16, F20, J16	GND		Ground
J20, L18, M16	GND		Ground

(To be continued…)

Pin	Signal	CPU Ball #	Description
M20, P18, R16	GND		Ground
R20, V12, V20	GND		Ground
Y18, AA14, AA17	GND		Ground
AA19, AA22, AB15	GND		Ground
AB21, A4, A7, A10	GND		Ground
B2, B5, B8, B9, C11	GND		Ground
D1, D5, D8, E2, H2	GND		Ground
H4, L2, L4, P2, P4	GND		Ground
R1, U2, U4, V1, W3	GND		Ground
Y2, AA1, AA4, AA7	GND		Ground
AA8, AA10, AA11	GND		Ground
AB3, AB6, AB9, AC4	GND		Ground
AC7, AC10, A26	GND		Ground
A29, A32, B27, B28	GND		Ground
B30, B33, C25, C32	GND		Ground
C35, D28, D34, F33	GND		Ground
F35, G34, H32, J33	GND		Ground
J35, K34, M35, N34	GND		Ground
T34, W34, AA25	GND		Ground
AA26, AA27, AA28	GND		Ground
AA32, AB28, AB31	GND		Ground
AB34, AC27, AC30	GND		Ground
AC33, AE2, AE34	GND		Ground
AF35, AG3, AH2	GND		Ground
AH34, AJ35, AK3	GND		Ground
AL2, AL34, AM13	GND		Ground
AM16, AM19, AN3	GND		Ground
AM22, AM35, AN6	GND		Ground
AN9, AN11, AN15	GND		Ground
AN18, AN21, AN33	GND		Ground
AP2, AP5, AP8	GND		Ground
AP13, AP16, AP19	GND		Ground
AP22, AP25, AP28	GND		Ground
AP31, AP34, AR14	GND		Ground
AR17, AR20, AR26	GND		Ground
AR29, AR32	GND		Ground
T18, T19, Y13, Y14	NC		No connection

Pin	Signal	CPU Ball #	Description
AP22, AP25, AP28	GND		Ground
AP31, AP34, AR14	GND		Ground
AR17, AR20, AR26	GND		Ground
AR29, AR32	GND		Ground
C2	MIPI_MCLK	AC9	Camera reference clock / GPIO
G3	MIPI_CAM_PWDN	AF11	Camera power down control / GPIO
G4	MIPI_CAM_RST	AG11	Camera interrupt signal input
B3	CSI_CKN	A16	MIPI CSI differential clock -
B4	CSI_CKP	B16	MIPI CSI differential clock +
C1	CSI_DN0	A14	MIPI CSI differential data lane 0 -
B1	CSI_DP0	B14	MIPI CSI differential data lane 0 +
A2	CSI_DN1	A15	MIPI CSI differential data lane 1 -
A3	CSI_DP1	B15	MIPI CSI differential data lane 1 +
A5	CSI_DN2	A17	MIPI CSI differential data lane 2 -
A6	CSI_DP2	B17	MIPI CSI differential data lane 2 +
B6	CSI_DN3	A18	MIPI CSI differential data lane 3 -
B7	CSI_DP3	B18	MIPI CSI differential data lane 3 +
C4	I2C3_SCL	E10	I^2C serial clock
C3	I2C3_SDA	F10	I^2C serial data
F4	LCD_BL_EN	AB15	1.8V backlight enable for MIPI DSI display / GPIO
E18	BL_PWM	AF14	MIPI DSI display backlight PWM dimming
F3	LCD_3V3_EN	E13	**3.3V** power enable for MIPI DSI display / GPIO
AB8	DSI_CKN	A11	MIPI DSI differential clock -
AB7	DSI_CKP	B11	MIPI DSI differential clock +
AB11	DSI_D0N	A9	MIPI DSI differential lane 0 -
AB10	DSI_D0P	B9	MIPI DSI differential lane 0 +
AC9	DSI_D1N	A10	MIPI DSI differential lane 1 -
AC8	DSI_D1P	B10	MIPI DSI differential lane 1 +
AC6	DSI_D2N	A12	MIPI DSI differential lane 2 -
AC5	DSI_D2P	B12	MIPI DSI differential lane 2 +
AB5	DSI_D3N	A13	MIPI DSI differential lane 3 -
AB4	DSI_D3P	B13	MIPI DSI differential lane 3 +
AA3	LCD_ID	P23	LCD panel identification / GPIO
M18, N18, AC18	NC		No connection
R19	JTRST	C27	JTAG test reset, active low. Not recommended to use
P19	NC		No connection
N17	JTCK	F26	JTAG clock. Not recommended to use.

(To be continued…)

Pin	Signal	CPU Ball #	Description
P17	JTDI	E27	JTAG data input. Not recommended to use.
R17	JTDO	E26	JTAG data output. Not recommended to use.
N19	JTMS	F27	JTAG mode select. Not recommended to use
C18, B22, C16, P16	NC		No connection
D6, D7, Y29, Y30	NC		No connection
Y31, AA29, AA30	NC		No connection
AA31, AK32, AK33	NC		No connection
AL32, AL33, AM32	NC		No connection
AM33, H18, J18	NC		No connection
K18, AB17, AC17	NC		No connection
AB19, AC19, D16	NC		No connection
C14	UART3_CTS	A7	UART3 clear to send
C13	UART3_RTS	B6	UART3 request to send
A14	UART3_RXD	D6	UART3 receive data
B13	UART3_TXD	B7	UART3 transmit data
D22	UART2_RXD	F15	UART2 debug port data input
D23	UART2_TXD	E15	UART2 debug port data output
V21	SAI5_RXD0	AD18	I^2S A digital audio input
W21	SAI5_TXD0	AC13	I^2S A digital audio output
V19	SAI5_RXD1	AC6	I^2S B digital audio input
W19	SAI5_TXD1	AF20	I^2S B digital audio output
W20	SAI5_BCLK	AD13	I^2S digital audio clock
W18	SAI5_LCLK	AC14	I^2S left-right channel synchronization clock
V18	SAI5_MCLK	AD15	I^2S master clock output
AB2	PCIE_RXN	A20	PCIe 2.0 data receive -
AB1	PCIE_RXP	B20	PCIe 2.0 data receive +
AC3	PCIE_TXN	A19	PCIe 2.0 data transmit -
AC2	PCIE_TXP	B19	PCIe 2.0 data transmit +
V2	PCIE20_PERST	AF17	PCIe 2.0 PHY reset
W2	PCIE20_CLKREQ	D13	PCIe 2.0 clock request
Y1	PCIEG2_CLK_N	A21	PCIe 2.0 clock transmit -
W1	PCIEG2_CLK_P	B21	PCIe 2.0 clock transmit +

Pin	Signal	CPU Ball #	Description
AA15	I2C2_SCL	D10	I^2C 2 serial clock
AA16	I2C2_SDA	D9	I^2C 2 serial data
AA20	I2C3_SCL	E10	I^2C 3 serial clock
AA21	I2C3_SDA	F10	I^2C 3 serial data
AB13	OTG1_DN	A22	USB2.0 OTG data -
AC14	OTG1_DP	B22	USB2.0 OTG data +
AC16	OTG1_EN	N24	USB2.0 OTG power enable
AB14	OTG1_ID	D22	USB2.0 OTG ID, high for device mode, low for host mode
AC15	OTG1_OC	AD9	USB2.0 OTG over-current, active low
AB16	USB1_VBUS	F22	USB2.0 OTG VBUS power detection
AB23	USB2_DN	A23	USB 2.0 host data -
AC22	USB2_DP	B23	USB 2.0 host data +
AC20	OTG1_DRV	AB10	USB2.0 OTG VBUS output driver enable
AB22	USB2_ID	D23	USB2.0 host insertion detection
J21	SD2_nCD	AA26	SDIO card detection
F21	SD2_CLK	W23	SDIO clock
E20	SD2_CMD	W24	SDIO command/response
G20	SD2_DATA0	AB23	SDIO data line 0
G21	SD2_DATA1	AB24	SDIO data line 1
H20	SD2_DATA2	V24	SDIO data line 2
H21	SD2_DATA3	V23	SDIO data line 3
C20	NVCC_SD2	PMIC_55	SDIO voltage
D21	SD2_nRST	AB26	SDIO power enable
D20	SD2_WP	AA27	SDIO write protect
D17	GPIO_A_0	AG16	GPIO_A_0
E17	GPIO_A_1	AB9	GPIO_A_1
F17	GPIO_A_2	AC18	GPIO_A_2
G17	GPIO_A_3	AB18	GPIO_A_3
H17	GPIO_A_4	AB19	GPIO_A_4
J17	GPIO_A_5	AD6	GPIO_A_5
D19	GPIO_B_0	AD19	GPIO_B_0
E19	GPIO_B_1	AC19	GPIO_B_1
F19	GPIO_B_2	AB22	GPIO_B_2
G19	GPIO_B_3	AC15	GPIO_B_3

(To be continued…)

Pin	Signal	CPU Ball #	Description
H19	GPIO_B_4	AG6	GPIO_B_4
J19	GPIO_B_5	AF6	GPIO_B_5
K19	GPIO_B_6	AG8	GPIO_B_6
L19	GPIO_B_7	AG7	GPIO_B_7
D3	GPIO_C_0	AG9	GPIO_C_0
D4	GPIO_C_1	AF9	GPIO_C_1
E3	GPIO_C_2	AF12	GPIO_C_2
E4	GPIO_C_3	AG10	GPIO_C_3
AF32	GPIO_E_0	K24	GPIO_E_0
AF33	GPIO_E_1	P26	GPIO_E_1
AG32	GPIO_E_2	R24	GPIO_E_2
AG33	GPIO_E_3	AF7	GPIO_E_3
AH32	GPIO_E_4	N22	GPIO_E_4
AH33	GPIO_E_5	AF23	GPIO_E_5
AJ32	GPIO_E_6	K23	GPIO_E_6
AJ33	GPIO_E_7	K23	GPIO_E_7
Y15	CPU_SPI2_SS0	A6	SPI chip select
U16	CPU_SPI2_SCLK	E6	SPI serial clock
U15	CPU_SPI2_MISO	A8	SPI master in slave out
V15	CPU_SPI2_MOSI	B8	SPI master out slave in

Pin	Signal	CPU Ball #	Description
R15	ENET_RGMII_RXCLK	AE26	RGMII A receive clock
M15	ENET_RGMII_RXCTL	AF27	RGMII receive control
N15	ENET_RGMII_RXD2	AD26	RGMII A receive data 2
P15	ENET_RGMII_RXD3	AC26	RGMII A receive data 3
J15	ENET_RGMII_TXCLK	AG24	RGMII A transmit clock
K16	ENET_RGMII_TXCTL	AF24	RGMII transmit control
K15	ENET_RGMII_RXD0	AE27	RGMII A receive data 0
L15	ENET_RGMII_RXD1	AD27	RGMII A receive data 1
H15	ENET_RGMII_TXD0	AG26	RGMII A transmit data 0
G15	ENET_RGMII_TXD1	AF26	RGMII A transmit data 1
H16	ENET_RGMII_TXD2	AG25	RGMII A transmit data 2
G16	ENET_RGMII_TXD3	AF25	RGMII A transmit data 3
M17	VDD_1V8	PMIC_15	1.8V power of ENET
T16	ENET_MDC	AC27	MDIO clock
T15	ENET_MDIO	AB27	MDIO data
A15, A17, A18	GND		Ground
A19, A21, B15	GND		Ground
B16, B17, B18	GND		Ground
B19, B20, B21	GND		Ground
A16	ANT		Main antenna

* Apart from those specified here, any pins not included in these sheets are not connected.

Ordering Information

Ordering No.	Chipset	Memory	Storage	Description
VOSM800-L	NXP i.MX 8M Mini	2GB LPDDR4	16GB eMMC	MIPI DSI, UART, USB, I^2C, SPI, PCIe
VOSM800-H	NXP i.MX 8M Mini	4GB LPDDR4	64GB eMMC	
VT-SBC-VOSM800-EVB-L	NXP i.MX 8M Mini	2GB LPDDR4	16GB eMMC	VOSM800-L + carrier board, MIPI DSI/HDMI, UART, USB, I^2C
VT-SBC-VOSM800-EVB-H	NXP i.MX 8M Mini	4GB LPDDR4	64GB eMMC	VOSM800-H + carrier board, MIPI DSI/HDMI, UART, USB, I^2C

Packing List	
VOSM800 system-on-module	1

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