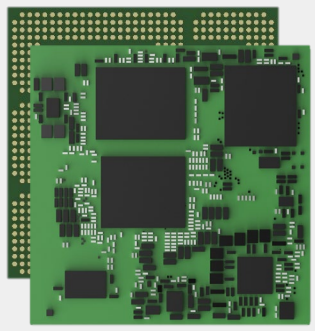
VOSM720 System-on-Module



Product Brief

The VOSM720 system-on-module is powered by the MediaTek MT8391 edge AI processor, which integrates an octa-core CPU, an Arm Mali-G57 MC2 GPU, and MediaTek's 8th-Gen NPU. It delivers up to 10 TOPS of computing power to accelerate advanced AI workloads—including object detection, image classification, speech recognition, and on-device generative AI and large language models (LLMs). The module supports 4K@30fps H.265/H.264 video encoding and 4K@60fps H.265/H.264/VP9 video decoding. Its robust display capabilities drive dual independent 2.5K60 screens or a single ultrawide 5K60 display, making it perfectly suitable for smart retail, digital kiosks, healthcare, and entertainment applications. The dual-camera ISP supports configurations of either a single 32MP or dual 16MP cameras, operating at 30 fps.

Connectivity options include Gigabit Ethernet on the module itself, with Wi-Fi and Bluetooth support on the carrier board. In addition, a comprehensive set of I/O ensures versatility for diverse IoT scenarios.

VOSM720 features LGA packaging that allows for direct welding, eliminating the need for additional connectors. Additionally, it is Open Standard Module (OSM) V1.1 compliant, enabling seamless integration into various products.

Features and benefits

VOSM720
High-performance, low-power edge AI processor
Up to 10 TOPS NPU for efficient real-time inference
4K@30 & 4K@60 H.265/H.264 encoder & decoder
Dual ISPs for single 32MP or dual 16MP cameras
Rich I/O: USB, UART, SPI, GPIO, PCIe, I2C, PWM
GbE on module, Wi-Fi & BT on the carrier board
Android and Yocto systems supported
OSM Size-L (45mm x 45mm) compliant
Extended service life (7+ years)

Application Scenarios

Smart Cities

AIDC (handheld)

Industrial HMI

Smart Home

Industrial IoT

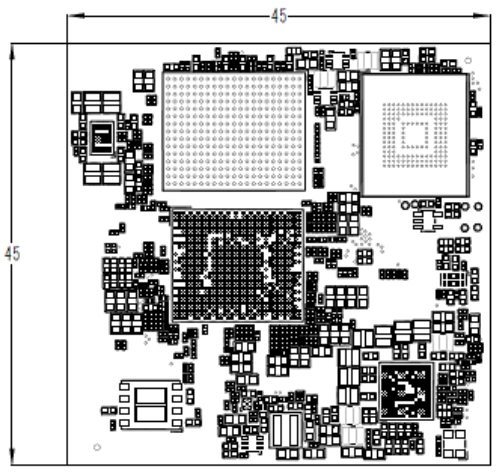
Smart Retail

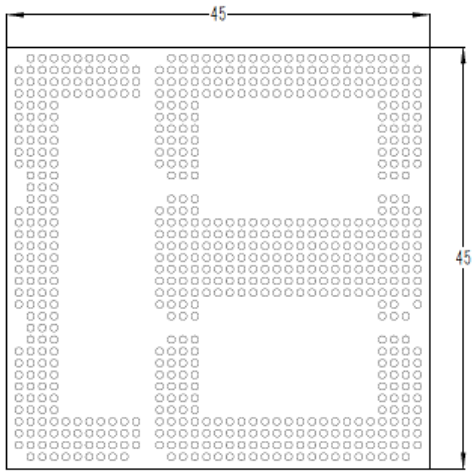
VOSM720 System-on-Module Datasheet

Specifications			
System	CPU	MediaTek MT8391 (G720), Dual-core Arm Cortex-A78 (2.4~2.6GHz), Hexa-core Arm Cortex-A55 (2.0GHz)	
	GPU	Arm Mali G57 MC2 GPU, 1.1GHz, Supports OpenGL ES 3.2, Vulkan 1.1, OpenCL 2.2	
	NPU	MediaTek 8th-Gen NPU (MDLA5.3, GenAI), Up to 10 TOPS	
	Memory	8GB LPDDR5	
	Storage	64GB UFS 3.1 (Optional: 128GB)	
Communication	Ethernet	GbE MAC (TSN)	
Media	Video processing	4K @30fps, H.265/H.264 video encoder	4K@60fp, H.265/H.264/VP9 video decoder
	Image processing	2 x ISP (3A, NR, AI-FD, LSC, Warp Engine) Single camera: 32MP @30fps, Dual camera: 16MP + 16MP@30fps	
Power	Input	5V/2A DC input	
	Consumption	Idle current: 130mA @5V DC	Operating current: 600mA @5V DC
Miscellaneous	RTC	Supported	
Software	Operating system	Android, Linux Yocto	
	Device management	BlueSphere MDM (Optional for Android version)	
Mechanical	Dimensions	45mm x 45mm (OSM Size-L)	Packaging: LGA
Environmental Condition	Temperature	Operating: -20℃ ~ +60℃ (Optional: -40℃ ~ +80℃)	Storage: -40℃ ~ +80℃
	Humidity	5%~95% RH (Non-condensing)	

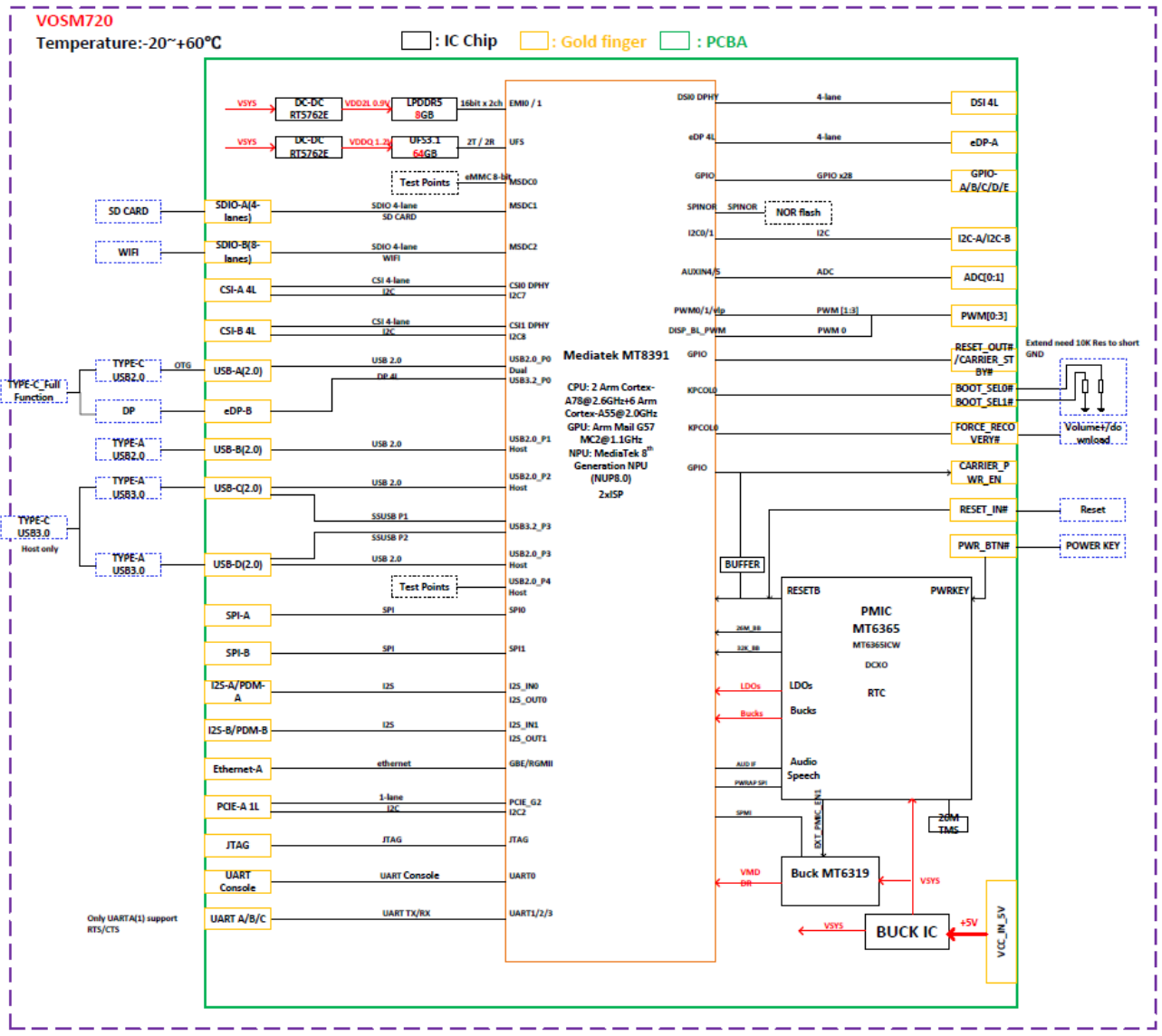
I/O			
Display (Dual display support, up to 3840 x 2160@60Hz)	1 x 4-Lane MIPI DSI, up to 5120 x 2160@60Hz / 2560 x 1600@120Hz		
	1 x 4-Lane eDP 1.4, up to 5120 x 2160@60Hz / 2560 x 1600@120Hz		
	1 x 4-Lane DP 1.4a/USB3.0 Host, up to 5120 x 2160@60Hz / 2560 x 1600@120Hz		
Camera	2 x 4-Lane MIPI CSI-2		
USB	1 x USB 3.0 Host, 1 x USB 3.0 Host/DP 1.4a	3 x USB 2.0 Host	1 x USB 2.0 OTG
ADC	2 x ADC input		
RGMII (Ethernet)	1 x RGMII/RMII		
PCIe	1 x 1-Lane PCIe 2.0		
SPI	2 x SPI		
Debug UART	1 x UART for debugging (1.8V level)		
Communication UART	3 x UART (1.8V level)		
I^2S	2 x I^2S		
I^2C	2 x I^2C		
PWM	3 x PWM		
GPIO	29 x GPIO (Max.)		
SDIO	2 x 4-Bit SDIO V3.0		
JTAG	Supported		
Button Signal	System reset, Forced recovery, Power on		

Product Outlines





Block Diagram



Electrical Characteristics

Absolute Maximum Ratings

Voltage beyond absolute maximum ratings may cause permanent damage to the module. Operation of the module outside of recommended conditions may result in reduced lifetime and/or reliability problems even if the absolute maximum ratings are not exceeded.

Parameter		Min.	Max.	Unit
Voltage of the SOM Module (VCC_IN_5V)		-0.3	5.5	V
Voltage of the RTC (SOM V_BAT)		-0.3	3.6	V
Voltage of the Carrier (VCC_IO_OUT)		-0.3	1.85	V
Voltage of LPDDR5 (x) DRAM	AVDD075_EMI	-	0.946	V
	AVDDQ_EMI	-	1.4	V
	VDD2H_EMI	-	1.4	V
	DVDD_DDRPHY	-	1.4	V
AVDD075_DRVDSI		-	0.825	V
AVDD12_AUXADC		-	1.32	V
AVDD12_CKSQ		-	1.32	V
AVDD12_CKBUF_UFS		-	1.32	V
AVDD12_CSI		-	1.32	V
AVDD12_DSI		-	1.32	V
AVDD12_EDPTX		-	1.32	V
AVDD12_PCIE		-	1.32	V
AVDD12_PLLGP_3H		-	1.32	V

Parameter	Min.	Max.	Unit
AVDD12_ PLLGP_4H	-	1.32	V
AVDD12_PLLGP_4H_APU	-	1.32	V
AVDD12_SSUSB_P1	-	1.32	V
AVDD12_SSUSB_P2	-	1.32	V
AVDD12_SSUSBDP_P1	-	1.32	V
AVDD12_SSUSBDP_P2	-	1.32	V
AVDD12_UFS_RX	-	1.32	V
AVDD12_UFS_TX	-	1.32	V
AVDD12_USB_P0	-	1.32	V
AVDD12_USB_P1	-	1.32	V
AVDD12_USB_P2	-	1.32	V
AVDD12_USB_P3	-	1.32	V
AVDD12_USB_P4	-	1.32	V
AVDD12_WBG	-	1.32	V
AVDD18_AUADC	-	1.98	V
AVDD18_AUXADC	-	1.98	V
AVDD18_CKSQ	-	1.98	V
AVDD18_DSI	-	1.98	V

(To be continued…)

Parameter	Min.	Max.	Unit
AVDD18_EDPTX	-	1.98	V
AVDD18_PCIE	-	1.98	V
AVDD18_PLLGP_3H	-	1.98	V
AVDD18_PLLGP_4H	-	1.98	V
AVDD18_PLLGP_4H_APU	-	1.98	V
AVDD18_PROC	-	1.98	V
AVDD18_SSUSB_P1	-	1.98	V
AVDD18_SSUSB_P2	-	1.98	V
AVDD18_SSUSBDP_P1	-	1.98	V
AVDD18_SSUSBDP_P2	-	1.98	V
AVDD18_USB_P0	-	1.98	V
AVDD18_USB_P1	-	1.98	V
AVDD18_USB_P2	-	1.98	V
AVDD18_USB_P3	-	1.98	V
AVDD18_USB_P4	-	1.98	V
AVDD18_UFS	-	1.98	V
AVDD18_VOWPLL	-	1.98	V
AVDD18_WBG	-	1.98	V
AVDD33_USB_L	-	3.22	V
AVDD33_USB_R	-	3.22	V
AVDD12_EMI	-	1.32	V
AVDD18_EMI	-	2.1	V
DVDD_APU	-	0.99	V
DVDD_CORE	-	0.88	V
DVDD_GPU	-	0.935	V
DVDD_PROC_B (power input for big core)	-	1.155	V
DVDD_PROC_L (power input for little core)	-	0.99	V
DVDD_SRAM_APU	-	0.99	V
DVDD_SRAM_CORE	-	0.88	V
DVDD_SRAM_GPU	-	0.935	V
DVDD_SRAM_VADSP	-	0.88	V
DVDD_SRAM_PROC_B	-	1.155	V
DVDD_SRAM_PROC_L	-	1.1	V
DVDD18_IOCAM	-	2.1	V
DVDD18_IOLEFT	-	2.1	V
DVDD18_IOBOT0	-	2.1	V
DVDD18_IORIGHT	-	2.1	V
DVDD18_IOPMIC	-	2.1	V
DVDD18_VQPS	-	1.98	V

Parameter	Min.	Max.	Unit
DVDD18_MSDC1	-	2.1	V
DVDD18_MSDC2	-	2.1	V
DVDD30_MSDC1	-	3.45	V
DVDD30_MSDC2	-	3.45	V

■ Recommended Operating Conditions

You are recommended to operate the module in the following conditions to achieve optimized performance of the module.

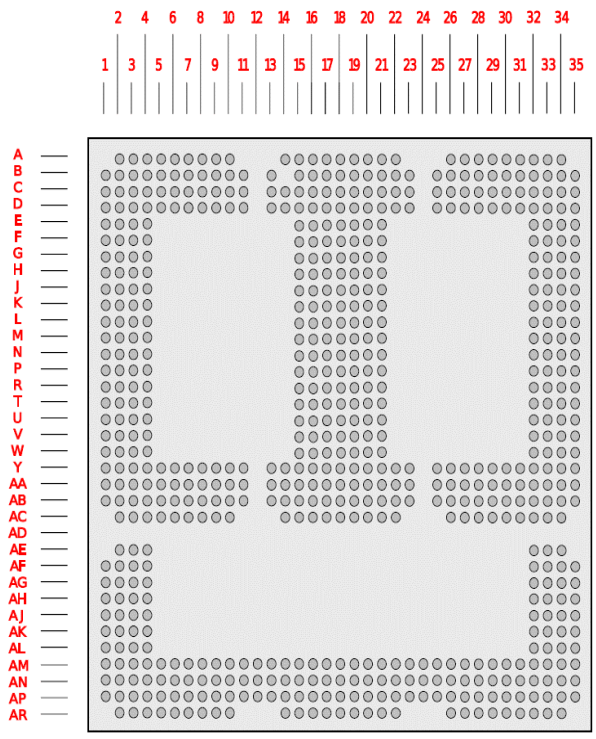
Parameter		Min.	Typ.	Max.	Unit
Voltage of the SOM Module (VCC_IN_5V)		4.8	5	5.2	V
Voltage of the RTC (SOM V_BAT)		2.2	3	3.6	V
Voltage of the Carrier (VCC_IO_OUT)		1.7	1.8	1.85	V
Voltage of LPDDR5 (x) DRAM	AVDD075_EMI	0.817	0.86	0.903	V
	AVDDQ_EMI	0.47	0.5	0.57	V
	VDD2H_EMI	1.01	1.05	1.12	V
	DVDD_DDRPHY	1.01	1.05	1.12	V
AVDD075_DRVDSI		0.7125	0.75	0.7875	V
AVDD12_AUXADC		1.14	1.2	1.26	V
AVDD12_CKSQ		1.14	1.2	1.26	V
AVDD12_CKBUF_UFS		1.14	1.2	1.26	V
AVDD12_CSI		1.14	1.2	1.26	V
AVDD12_DSI		1.14	1.2	1.26	V
AVDD12_EDPTX		1.14	1.2	1.26	V
AVDD12_PCIE		1.14	1.2	1.26	V
AVDD12_PLLGP_3H		1.14	1.2	1.26	V
AVDD12_ PLLGP_4H		1.14	1.2	1.26	V
AVDD12_PLLGP_4H_APU		1.14	1.2	1.26	V
AVDD12_SSUSB_P1		1.14	1.2	1.26	V
AVDD12_SSUSB_P2		1.14	1.2	1.26	V
AVDD12_SSUSBDP_P1		1.14	1.2	1.26	V
AVDD12_SSUSBDP_P2		1.14	1.2	1.26	V
AVDD12_UFS_RX		1.14	1.2	1.26	V
AVDD12_UFS_TX		1.14	1.2	1.26	V
AVDD12_USB_P0		1.14	1.2	1.26	V
AVDD12_USB_P1		1.14	1.2	1.26	V
AVDD12_USB_P2		1.14	1.2	1.26	V
AVDD12_USB_P3		1.14	1.2	1.26	V
AVDD12_USB_P4		1.14	1.2	1.26	V
AVDD12_WBG		1.14	1.2	1.26	V

(To be continued…)

Parameter		Min.	Typ.	Max.	Unit
AVDD18_AUADC		1.71	1.8	1.89	V
AVDD18_AUXADC		1.71	1.8	1.89	V
AVDD18_CKSQ		1.71	1.8	1.89	V
AVDD18_DSI		1.71	1.8	1.89	V
AVDD18_EDPTX		1.71	1.8	1.89	V
AVDD18_PCIE		1.71	1.8	1.89	V
AVDD18_PLLGP_3H		1.71	1.8	1.89	V
AVDD18_PLLGP_4H		1.71	1.8	1.89	V
AVDD18_PLLGP_4H_APU		1.71	1.8	1.89	V
AVDD18_PROC		1.71	1.8	1.89	V
AVDD18_SSUSB_P1		1.71	1.8	1.89	V
AVDD18_SSUSB_P2		1.71	1.8	1.89	V
AVDD18_SSUSBDP_P1		1.71	1.8	1.89	V
AVDD18_SSUSBDP_P2		1.71	1.8	1.89	V
AVDD18_USB_P0		1.71	1.8	1.89	V
AVDD18_USB_P1		1.71	1.8	1.89	V
AVDD18_USB_P2		1.71	1.8	1.89	V
AVDD18_USB_P3		1.71	1.8	1.89	V
AVDD18_USB_P4		1.71	1.8	1.89	V
AVDD18_UFS		1.71	1.8	1.89	V
AVDD18_VOWPLL		1.71	1.8	1.89	V
AVDD18_WBG		1.71	1.8	1.89	V
AVDD33_USB_L		2.92	3.07	3.22	V
AVDD33_USB_R		2.92	3.07	3.22	V
AVDD12_EMI		1.14	1.2	1.26	V
AVDD18_EMI		1.7	1.8	1.95	V
DVDD_SRAM_ADSP	Digital power input for ADSP	0.76	0.8	0.84	V
		0.71	0.75	0.7875	V
DVDD_APU	Digital power input for APU	0.855	0.9	0.945	V
		0.7125	0.75	0.7875	V
		0.5225	0.55	0.5775	V
DVDD_CORE	Digital power input for Vcore	0.76	0.8	0.84	V
		0.68875	0.725	0.76125	V
		0.6175	0.65	0.6825	V
		0.57	0.6	0.63	V
		0.5225	0.55	0.5775	V

Parameter		Min.	Typ.	Max.	Unit
DVDD_GPU	Digital power input for GPU	0.797	0.85	0.918	V
		0.703	0.75	0.81	V
		0.609	0.65	0.702	V
		0.539	0.575	0.621	V
DVDD_PROC_B	Digital power input for Big Core	0.9975	1.05	1.1025	V
		0.855	0.9	0.945	V
		0.7125	0.75	0.7875	V
		0.5225	0.55	0.5775	V
DVDD_PROC_L	Digital power input for Little Core	0.855	0.9	0.945	V
		0.7125	0.75	0.7875	V
		0.5225	0.55	0.5775	V
DVDD_SRAM_APU	Digital power input for APU SRAM	0.855	0.9	0.945	V
		0.7125	0.75	0.7875	V
DVDD_SRAM_CORE	Digital power input for Core SRAM	0.76	0.8	0.84	V
		0.7125	0.75	0.7875	V
DVDD_SRAM_GPU	Digital power input for GPU SRAM	0.797	0.85	0.918	V
		0.703	0.75	0.81	V
DVDD_SRAM_PROC_B	Digital power input for Big Core SRAM	0.9975	1.05	1.1025	V
		0.95	1	1.05	V
		0.7125	0.75	0.7875	V
DVDD_SRAM_PROC_L	Digital power input for Little Core SRAM	0.9975	1.05	1.1025	V
		0.95	1	1.05	V
		0.7125	0.75	0.7875	V
DVDD18_IOCAM		1.71	1.8	1.89	V
DVDD18_IOLEFT		1.71	1.8	1.89	V
DVDD18_IOBOT0		1.71	1.8	1.89	V
DVDD18_IORIGHT		1.71	1.8	1.89	V
DVDD18_IOPMIC		1.71	1.8	1.89	V
DVDD18_MSDC1		1.71	1.8	1.89	V
DVDD18_MSDC2		1.71	1.8	1.89	V
DVDD18_VQPS		1.71	1.8	1.89	V
DVDD3_MSDC1	Digital power input for MSDC1	1.71	1.8	1.89	V
		2.7	3	3.15	V
DVDD3_MSDC2	Digital power input for MSDC2	1.71	1.8	1.89	V
		2.7	3	3.15	V

Pinout



(View from top, through the module)

In the tables below:

* **Pin** refers to the pin number defined by OSM as shown in above figure.

* **Signal** refers to the pin name used by Vantron.

* **CPU Pad Name** refers to corresponding pad name on the MTK Genio 720 CPU.

* Certain signals are derived from additional ICs and the corresponding IC names are provided.

* Unless otherwise explicitly stated, the I/O level is **1.8V**.

Pin*	Signal*	CPU Pad Name*	Description
U19	BOOT_SEL0#		UFS: BOOT0-->L, BOOT1-->L SPI: BOOT0-->H, BOOT1-->L eMMC: BOOT0-->L, BOOT1-->H
R18	BOOT_SEL1#		
V17	CARRIER_PWR_EN	AE3	HW: SYSRSTB#; SW: CARRIER_PWR_EN_A (PU 1K)
T17	FORCE_RECOVERY#	AG5	FORCE_RECOVERY# (PU 10K)
AA9	PWR_BTN#	D8 (MT6365)	POWER KEY (**4.2V** voltage) 0=active; 1=in-active (PU 47K)
W17	RTC_PWR	L13 (MT6365)	RTC power input (**2.8V** voltage)
U17	SYS_RST#	CPU: AG6 / MT6365: E3	System reset
AB18, AA18	NC		No connection
M19	VCC_2_TEST	B13 (MT6365)	Digital power for CORE
Y16	VCC_3_TEST	H15, E15 (MT6365)	Digital power for SRAM_CORE
Y20	VCC_4_TEST	A8 (MT6365)	0.75V analog power for EMI
Y3	VCC_5_TEST	B15(MT6365)	Digital power for GPU
C5	VCC_6_TEST	A5, A2 (MT6365)	Digital power for PROC_B
AA33	VCC_7_TEST	B10 (MT6365)	Digital power for PROC_L
B29	VCC_8_TEST	L15 (MT6365)	Digital power for APU
Y17, Y8, Y9, Y10	VCC_IN_5V		**5V** power input for the module
Y11, Y25, Y26	VCC_IN_5V		**5V** power input for the module
Y27, Y28, AE4	VCC_IN_5V		**5V** power input for the module
AF4, AG4, AH3, AH4	VCC_IN_5V		**5V** power input for the module
AJ3, AJ4, AK4, Y19	VCC_IN_5V		**5V** power input for the module
U18	VCC_OUT_IO	R15 (MT6365)	1.8V IO power source output
D18, E15, E21, F16, F20, J16, J20, L18	GND		Ground
M16, M20, P18, R16, R20, V16, V20, Y18	GND		Ground
AA14, AA17, AA19, AA22, AB15, AB21	GND		Ground
A4, A7, A10, B2, B5, B8, B9, C11, D1, D5	GND		Ground
D8, E2, H2, H4, L2, L4, P2, P4, R1, U2	GND		Ground
U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10	GND		Ground
AA11, AB3, AB6, AB9, AC4, AC7, AC10	GND		Ground
A26, A29, A32, B27, B28, B30, B33, C25	GND		Ground
C32, C35, D28, D34, F33, F35, G34, H32	GND		Ground
J33, J35, K34, M35, N34, T34, W34, AA25	GND		Ground
AA26, AA27, AA28, AA32, AB28, AB31	GND		Ground
AB34, AC27, AC30, AC33, AE34, AE2	GND		Ground
AG3, AL2, AH2, AK3, AF35, AH34, AJ35	GND		Ground
AL34, AM13, AM16, AM19, AN3, AM22	GND		Ground
AM35, AN6, AN9, AN11, AN15, AN18	GND		Ground
AN21, AN33, AP13, AP2, AP5, AP8, AP16	GND		Ground
AP19, AP22, AP25, AP28, AP31, AP34	GND		Ground
AR14, AR17, AR20, AR26, AR29, AR32	GND		Ground
T18	I2S_B_LRCLK	AH5	I^2S B left/right clock
T19	I2S_B_BITCLK	AJ6	I^2S B bit clock
Y13	CARRIER_STBY#	AD14	Carrier board standby, active low
Y14	RESET_OUT#	AE14	Reset output, active low
AA13, AA2, N2	NC		No connection
J32	CSI_B_CLOCK_N	MIPI CSI voltage	J5	MIPI CSI B clock -
K32	GND			Ground
K33	CSI_B_CLOCK_P	MIPI CSI voltage	J6	MIPI CSI B clock +
L32	CSI_B_DATA0_N		J7	MIPI CSI B differential data 0 -
M32	GND			Ground
M33	CSI_B_DATA0_P	MIPI CSI voltage	H6	MIPI CSI B differential data 0 +
N32	CSI_B_DATA1_N		J2	MIPI CSI B differential data 1 -
P32	CSI_B_DATA1_P		J1	MIPI CSI B differential data 1 +

(To be continued…)

Pin	Signal	CPU Pad Name		Description
P34	CSI_B_DATA2_N	MIPI CSI voltage	H7	MIPI CSI B differential data 2 -
R32	GND			Ground
R33	CSI_B_DATA2_P	MIPI CSI voltage	H8	MIPI CSI B differential data 2 +
T32	CSI_B_DATA3_N		J3	MIPI CSI B differential data 3 -
T33	CSI_B_DATA3_P		J4	MIPI CSI B differential data 3 +
AB25	CAM_B_SCL	G4		Camera B serial clock
AB26	CAM_B_SDA	G3		Camera B serial data
AE32, AL3, AL4, AM3, AM4, AM5	NC			No connection
AM6, AM7, AM10, AM8, AM9, AM23	NC			No connection
AM24, AM25, AM26, AM27	NC			No connection
AM28, AM29, AM30, AM31, AN2	NC			No connection
AN5, AN7, AN8, AN24 AN25, AN26	NC			No connection
AN27, AN28, AN29, AN30, AN31, AP10	NC			No connection
AP22, AP25, AP28, AP31, AP34, AR14	GND			Ground
AR17, AR20, AR26, AR29, AR32	GND			Ground
C2	CAM_MCLK	F5		Camera main clock
G3	CAM_A_PWR	AF17		Camera A power (out)
G4	CAM_A_RST#	AF16		Camera A reset, active low
B3	CSI0A_L2P_T1C	MIPI CSI voltage	L4	MIPI CSI A clock -
B4	CSI0A_L2P_T1B		K4	MIPI CSI A clock +
C1	CSI0A_L0P_T1A		K3	MIPI CSI A differential data 0 -
B1	CSI0A_L0P_T0C		L6	MIPI CSI A differential data 0 +
A2	CSI0B_L0N_T0B		M5	MIPI CSI A differential data 1 -
A3	CSI0B_L0P_T0A		L5	MIPI CSI A differential data 1 +
A5	CSI0A_L0N_T0B		L7	MIPI CSI A differential data 2 -
A6	CSI0A_L0P_T0A		K7	MIPI CSI A differential data 2 +
B6	CSI0B_L1N		M3	MIPI CSI A differential data 3 -
B7	CSI0B_L1P_T0C		M4	MIPI CSI A differential data 3 +
C4	CAM_A_SCL	G1		Camera A serial clock (PU 2.2K)
C3	CAM_A_SDA	G2		Camera A serial data (PU 2.2K)
F4	DISP_BL_EN	AF8		Backlight enable for MIPI DSI display (PD)
E18	DISP_BL_PWM	AB32		PWM dimming for MIPI DSI display (PD)
F3	DISP_VDD_EN	AD6		VDD logic enable for MIPI DSI display (PD)
AB8	DSI_CKN_T1C	MIPI DSI voltage	W30	MIPI DSI clock -
AB7	DSI_CKP_T1B		W31	MIPI DSI clock +
AB11	DSI_D0N_T1A		W32	MIPI DSI differential data 0 -
AB10	DSI_D0P_T0C		Y30	MIPI DSI differential data 0 +
AC9	DSI_D1N_T2B		V33	MIPI DSI differential data 1 -
AC8	DSI_D1P_T2A		V34	MIPI DSI differential data 1 +
AC6	DSI_D2N_T0B		Y31	MIPI DSI differential data 2 -
AC5	DSI_D2P_T0A		Y29	MIPI DSI differential data 2 +
AB5	DSI_D3N		V29	MIPI DSI differential data 3 -
AB4	DSI_D3P_T2C		V30	MIPI DSI differential data 3 +

Pin	Signal	CPU Pad Name	Description
AA3	DSI_TE	AB28	Tearing effect (TE) of MIPI DSI display (PD)
M18	ADC_0	V6	ADC input 0
N18	ADC_1	V7	ADC input 1
AC18	NC		No connection
R19	JTAG_nTRST	AG12	JTAG test reset (PU)
P19	NC		No connection
N17	JTAG_TCK	AD13	JTAG test clock (PD)
P17	JTAG_TDI	AF12	JTAG test data in (PD)
R17	JTAG_TDO	AD12	JTAG test data out (PD)
N19	JTAG_TMS	AE12	JTAG test mode select (PD)
C18	NC		No connection
B22, C16, P16, D6	NC		No connection
D7, Y29, Y30, Y31	NC		No connection
AA29, AA30, AA31	NC		No connection
AK32, AK33, AL32	NC		No connection
AL33, AM32, AM33	NC		No connection
F18	PWM_1	AF14	Pulse width modulation 1
G18	PWM_2	AG14	Pulse width modulation 2
H18	PWM_3	AF3	Pulse width modulation 3
J18, K18, AB17	NC		No connection
AC17, AB19, AC19	NC		No connection
C14	UART_A_CTS	AG11	UART A clear to send (PD)
C13	UART_A_RTS	AF11	UART A request to send (PD)
A14	UART_A_RX	AJ12	UART A receive data (PD)
B13	UART_A_TX	AH12	UART A transmit data (PD)
D16, D15	NC		No connection
D14	UART_B_RXD	AE11	UART B receive data (PD)
D13	UART_B_TXD	AD11	UART B transmit data (PD)
A22	UART_C_RX	AC4	UART C receive data (PD)
B23	UART_C_TX	AC3	UART C transmit data (PD)
D22	UART_CON_RX	AH10	UART console receive (PU)
D23	UART_CON_TX	AH11	UART console transmit (PU)
C22, C23, M34	NC		No connection
V21	I2S_A_DATA_IN	AH9	I^2S A data input
W21	I2S_A_DATA_OUT	AF9	I^2S A data output
V19	I2S_B_DATA_IN	AH4	I^2S B data input
W19	I2S_B_DATA_OUT	AE19	I^2S B data output
W20	I2S_A_BITCLK	AH8	I^2S A bit clock
W18	I2S_A_LRCLK	AH7	I^2S A left/right clock
V18	I2S_MCLK	AJ7	I^2S master clock
AB2	PCIe_A_HSI0_N	PCIe voltage N27	PCIe A receive data 0 –
AB1	PCIe_A_HSI0_P	N28	PCIe A receive data 0 +
AC3	PCIe_A_HSO0_N	N32	PCIe A transmit data 0 -
AC2	PCIe_A_HSO0_P	N31	PCIe A transmit data 0 +
V2	PCIe_A_PERST#	AB30	PCIe A reset, active low
L34, L35, K35, L33	PCIe_A_HSI0_N		No connection

(To be continued…)

Pin	Signal	CPU Pad Name		Description
W2	PCIe_CLKREQ#	AB29		PCIe clock request, active low (PU 10K)
Y1	PCIe_A_REFCLK_N	M34		PCIe 1 reference clock – (PD 49.9R)
W1	PCIe_A_REFCLK_P	M33		PCIe 1 reference clock + (PD 49.9R)
R2	PCIE_SM_ALERT#	AC6		PCIe 1 wakeup, active low (PD)
T1	PCIe_SMCLK	AG17		USB 0 high-speed data – (PU 2.2K)
U1	PCIe_SMDAT	AE17		USB 0 high-speed data + (PU 2.2K)
T2	PCIe_WAKE#	AB31		USB-C VBUS enable (PU 10K)
D11	USB_C_DN	USB voltage	AF28	USB C data -
D10	USB_C_DP		AF29	USB C data +
C10	USB_C_EN	AE2		USB C enable
D9, C8	NC			No connection
B11	SSUSB_RXN_P1	USB voltage	AE30	USB C super-speed receive data -
B10	SSUSB_RXP_P1		AE31	USB C super-speed receive data +
A9	SSUSB_TXN_P1		AF32	USB C super-speed transmit data -
A8	SSUSB_TXP_P1		AF33	USB C super-speed transmit data +
C9	NC			No connection
D26	USB_DM_P2	USB voltage	W1	USB D data -
D25	USB_DP_P2		W2	USB D data +
C26	USB_D_EN	AC2		USB D enable
D27, C28, C27	NC			No connection
AA15	I2C_A_SCL	AG7		I^2C A serial clock (PU 2.2K)
AA16	I2C_A_SDA	AE7		I^2C A serial data (PU 2.2K)
AA20	I2C_B_SCL	AF7		I^2C B serial clock (PU 2.2K)
AA21	I2C_B_SDA	AD7		I^2C B serial data (PU 2.2K)
AB13	USB_A_DN	USB voltage	R3	USB A data -
AC14	USB_A_DP		P3	USB A data +
AC16	USB_A_EN	AH17		USB A enable
AB14	USB_A_ID	AJ16		USB A OTG ID
AC15, AB22, AC21, AB20	NC			No connection
AB16	USB_A_VBUS			USB A VBUS **(5V)**
AB23	USB_B_DN	USB voltage	U3	USB B data -
AC22	USB_B_DP		V3	USB B data +
AC20	USB_B_EN	AC1		USB B enable
AB22, AC21, AB20	NC			No connection
J21	SDIO_A_CD#	AE5		SDIO A card detect, active low (PD)
F21	SDIO_A_CLK	AH2		SDIO A clock (PD)
E20	SDIO_A_CMD	AG2		SDIO A command (PD)
G20	SDIO_A_DAT0	AH3		SDIO A data 0 (PD)
G21	SDIO_A_DAT1	AG3		SDIO A data 1 (PD)
H20	SDIO_A_DAT2	AF1		SDIO A data 2 (PD)
H21	SDIO_A_DAT3	AG1		SDIO A data 3 (PD)
C20	VSIM1_PMU	P8 (MT6365)		SIM1 power supply (**1.8V/3.3V**)
D21	SDIO_A_PWR_EN	AD4		SDIO A power enable (**3.0V**)

Pin	Signal	CPU Pad Name	Description
D20, T21	NC		No connection
K20	SDIO_B_CLK	E1	SDIO B clock (PD)
K21	SDIO_B_CMD	E2	SDIO B command (PD)
L20	SDIO_B_DAT0	E3	SDIO B data 0 (PD)
L21	SDIO_B_DAT1	F3	SDIO B data 1 (PD)
M21	SDIO_B_DAT2	C2	SDIO B data 2 (PD)
N20	SDIO_B_DAT3	D2	SDIO B data 3 (PD)
N21, P20, P21	NC		No connection
R21, T20, U20	NC		No connection
U21	SDIO_B_RST#	AC8	SDIO B reset, active low
D17	GPIO_A_0	AE1	GPIO
E17	GPIO_A_1	AE6	GPIO
F17	GPIO_A_2	AE4	GPIO
G17	GPIO_A_3	AD5	GPIO
H17	GPIO_A_4	AF2	GPIO
J17	GPIO_A_5	AG4	GPIO
D19	GPIO_B_0	AF4	GPIO
E19	GPIO_B_1	AG8	GPIO
F19	GPIO_B_2	AF13	GPIO
G19	GPIO_B_3	F6	GPIO
H19	GPIO_B_4	AG18	GPIO
J19	GPIO_B_5	AF18	GPIO
K19	GPIO_B_6	AH18	GPIO
L19	GPIO_B_7	AJ18	GPIO
D3	GPIO_C_0	AH6	GPIO
D4	GPIO_C_1	AE13	GPIO
E3	CAM_B_PWR	AC5	Camera B power
E4	eDP_BLK_EN	AB5	eDP backlight enable
U32	GPIO_D_0	F7	GPIO
U33	GPIO_D_1	AJ9	GPIO
V32	GPIO_D_2	AG9	GPIO
V33	GPIO_D_3	AJ10	GPIO
W32	GPIO_D_4	AD16	GPIO
W33	GPIO_D_5	AE16	GPIO
Y32	GPIO_D_6	AC32	GPIO
AF32	GPIO_E_0	AB33	GPIO
AF33	GPIO_E_1	AB34	GPIO
AG32	GPIO_E_2	AF17	GPIO
AG33	GPIO_E_3	AF16	GPIO
AH32	GPIO_E_4	AC20	GPIO
AH33	GPIO_E_5	AF20	GPIO
AJ32, AJ33, W15, W16, K17, L17	NC		No connection
Y15	SPI_A_CS0#	AG15	SPI A chip select, active low (PD)
U16	SPI_A_SCK	AF15	SPI A serial clock (PD)
U15	SPI_A_SDI	AE15	SPI A serial data in (PD)
V15	SPI_A_SDO	AD15	SPI A serial data out (PD)

(To be continued…)

Pin	Signal	CPU Pad Name	Description
AA23	SPI_B_CS0#	AH15	SPI B chip select, active low
Y21	SPI_B_SCK	AJ15	SPI B serial clock (PD)
Y22	SPI_B_SDI	AH14	SPI B serial data in (PD)
Y23	SPI_B_SDO	AH13	SPI B serial data out (PD)
C30, Y33, D29, C29, D30, E16	NC		No connection
F15	GBE_COL	J24	Gigabit Ethernet collision
R15	ETH_A_RGMII_RX_CLK	AG20	Ethernet A RGMII receive clock
M15	ETH_A_RGMII_RX_DV	AE20	Ethernet A RGMII receive data valid
L16	ETH_A_RGMII_RX_ER	AD20	Ethernet A RGMII receive error
N15	ETH_A_RGMII_RXD2	AG21	Ethernet A RGMII receive data 2
P15	ETH_A_RGMII_RXD3	AF21	Ethernet A RGMII receive data 3
J15	ETH_A_RGMII_TX_CLK	AJ19	Ethernet A RGMII transmit clock
K16	ETH_A_RGMII_TX_EN	AH19	Ethernet A RGMII transmit enable
K15	ETH_A_RGMII_RXD0	AC21	Ethernet A RGMII receive data 0
L15	ETH_A_RGMII_RXD1	AD21	Ethernet A RGMII receive data 1
H15	ETH_A_RGMII_TXD0	AH20	Ethernet A RGMII transmit data 0
G15	ETH_A_RGMII_TXD1	AH21	Ethernet A RGMII transmit data 1
H16	ETH_A_RGMII_TXD2	AJ21	Ethernet A RGMII transmit data 2
G16	ETH_A_RGMII_TXD3	AJ22	Ethernet A RGMII transmit data 3
N16	ETH_A_PPS	AC19	Ethernet A pulse per second
E1, D2, P1, L1, K2	NC		No connection
M1, N1, H1, J2, J1	NC		No connection

Pin	Signal	CPU Pad Name		Description
K1, G1, F1, G2, F2	NC			No connection
C6, C7, M2, AB35	NC			No connection
C34	eDP0_AUX_M	P29		eDP 0 auxiliary channel - (PU 100K)
C33	eDP0_AUX_P	P30		eDP 0 auxiliary channel + (PD 100K)
D31	eDP_A_BL_EN	AD8		eDP A backlight enable
D33	eDP_A_BL_HPD	AD18		eDP A backlight hot-plug detection (PD 1M)
C31	eDP_A_BL_PWM	AD19		eDP A backlight PWM control
A31	eDP_LN0_TXN	eDP HBR2/3 voltage	R28	eDP 0 transmit lane 0 -
A30	eDP_LN0_TXP		R27	eDP 0 transmit lane 0 +
B32	eDP_LN1_TXN		T29	eDP 0 transmit lane 1 -
B31	eDP_LN1_TXP		T30	eDP 0 transmit lane 1 +
A34	eDP_LN2_TXN		R31	eDP 0 transmit lane 2 -
A33	eDP_LN2_TXP		R32	eDP 0 transmit lane 2 +
B35	eDP_LN3_TXN		U32	eDP 0 transmit lane 3 -
B34	eDP_LN3_TXP		U31	eDP 0 transmit lane 3 +
H33	DP_AUX-	R7		DP auxiliary channel – (PD 100K)
G33	DP_AUX+	R8		DP auxiliary channel + (PD 100K)
G32	DP_TX_HPD	AC18		DP hot plug detect (PD 1M)
E35	DP_D0-	T1		DP lane 0 data -
D35	DP_D0+	T2		DP lane 0 data +
F34	DP_D1-	T5		DP lane 1 data -
E34	DP_D1+	T4		DP lane 1 data +
H35	DP_D2-	P6		DP lane 2 data -
G35	DP_D2+	P5		DP lane 2 data +
J34	DP_D3-	N7		DP lane 3 data -
H34	DP_D3+	N8		DP lane 3 data +

* Apart from those specified here, any pins not included in these sheets are not connected.

Ordering Information

Nomenclature: VOSM720-[OS-S-T]

OS (Operating System): **A** – Android; **Y** – Yocto

S (Storage): L – 64GB UFS; **H** – 128GB UFS

T (Temperature): **D –** -20℃ ~ +60℃; **E –** -40℃ ~ +80℃

Example Ordering No.	Operating system	Memory	Storage	Temperature Range	Packaging
VOSM720-ALD	Android	4GB LPDDR5	64GB UFS	-20℃ ~ +60℃	LGA
VOSM720-YHE	Yocto	4GB LPDDR5	128GB UFS	-40℃ ~ +80℃	LGA
VT-SBC-VOSM720-EVB	VOSM720 + Carrier board				

Packing List	
VOSM720 system-on-module	1