VOSM700 System-on-Module

Product Brief

The VOSM700 system-on-module is powered by the MediaTek MT8390 chipset, featuring an octa-core high-performance CPU, an Arm Mali-G57 MC2 GPU that supports up to dual 4K display and 4K video CODEC, and a 5th-Gen NPU delivering up to 4 TOPS of computing power for AI inference. The HiFi 5 audio DSP offers efficient pre-/post-processing capability for audio and video contents. The dual-camera ISP supports configurations of a single 32MP camera, operating at 30 fps.

The module boasts versatile I/O options, including PCIe 2.0, USB, and multiple UART, I2C, SPI, and GPIO connections. With support for Wi-Fi and Bluetooth connectivity, as well as a GbE MAC with TSN, it is well suited for diverse application scenarios.

VOSM700 features LGA packaging that allows for direct welding, eliminating the need for additional connectors. Furthermore, its compliance with the Open Standard Module (OSM) V1.1 standard ensures seamless integration into various products. The module is designed to support an extensive range of IoT applications, such as smart home, industrial automation, healthcare, and smart cities, ensuring high levels of security, robust performance, and versatile flexibility.

Features and benefits

VOSM700
High-performance, low-power edge AI processor
Up to 4 TOPS NPU for AI acceleration
HiFi 5 audio DSP, 4K video CODEC
Dual ISPs for single 32MP camera
Rich interfaces, robust system performance
Wi-Fi & Bluetooth integrated; RF ready
Android and Linux Yocto support
OSM Size-L (45mm x 45mm) compliant
Extended service life (7+ years)

Application Scenarios

Smart Cities

Healthcare

Fitness Console

Home Appliance

Industrial IoT

Smart Retail

VOSM700 System-on-Module Datasheet

Specifications			
System	CPU	MediaTek MT8390, Dual-core ARM Cortex-A78 (2.2GHz) + Hexa-core ARM Cortex-A55 (2.0GHz)	
	GPU	Arm Mali-G57 MC3 GPU, 950MHz, Supports OpenGL ES 3.2, Vulkan 1.1, OpenCL 2.2	
	NPU	MediaTek 5th-Gen NPU (MDLA3.0 + Tensilica VP6), 4.0 TOPS	
	Memory	4GB 64-bit LPDDR4x	
	Storage	64GB eMMC 5.1	
	EEPROM	2Kb (for hardware configuration information)	
Communication	Wi-Fi	IEEE 802.11 a/b/g/n/ac	
	Bluetooth	Bluetooth 5.2	
Media	Video processing	4K @30Hz, H.265/H.264 video encoding	4K @75Hz, H.265/H.264/VP9/AV1 video decoding
	Audio DSP	Tensilica HiFi 5	
	Camera ISP	2 x ISP (3A, NR, AI-FD, LSC, HDR, Warp Engine); Single camera: 32MP @30fps	
Power	Input	5V/1A DC input	
Software	Operating system	Android, Linux Yocto	
	Device management	BlueSphere MDM (Optional for Android version)	
Mechanical	Dimensions	45mm x 45mm (OSM Size-L)	Packaging: LGA
Environmental Condition	Temperature	Operating: -20℃ ~ +60℃ Optional: -40℃ ~ +80℃	Storage: -40℃ ~ +80℃
	Humidity	5%~95% RH (Non-condensing)	

I/O		
Display (Dual display support)	1 x 4-Lane MIPI DSI, up to 2K@30Hz	1 x 4-Lane DP, up to 4K@60Hz
	1 x 2-Lane eDP, up to 2560 x 1600@60Hz	1 x HDMI, up to 4K@60Hz
MIPI CSI	1 x 4-Lane MIPI CSI	
ADC	2 x ADC	
Ethernet	1 x RGMII	
Audio	2 x Audio output (Support 1 x Headphone/Speaker, 1 x Speaker)	
	2 x Audio input (Support dual-Mic/headphone-Mic or digital Mic)	
SPI	3 x SPI	
Debug UART	1 x UART for debugging (1.8V level)	
Communication UART	2 x UART for communication (1.8V level)	
I^2S	1 x I^2S	
I^2C	2 x I^2C	
PWM	2 x PWM	
USB	2 x USB 2.0 OTG	1 x USB 3.0
GPIO	33 x GPIO (Max.)	
PCIe	1 x 1-Lane PCIe 2.0	
SDIO	1 x 4-bit SDIO 3.0	
JTAG	Supported	
Key Signal	Support 1 x Recovery key, 1 x Power key, 1 x Reset key	

Electrical Characteristics

Absolute Maximum Ratings

Voltage beyond absolute maximum ratings may cause permanent damage to the module. Operation of the module outside of recommended conditions may result in reduced lifetime and/or reliability problems even if the absolute maximum ratings are not exceeded.

Parameter		Min.	Max.	Unit
Voltage of the SOM		0	5	V
Voltage on Wi-Fi/BT chip	AVDD18	-0.3	1.98	V
	AVDD33	-0.3	3.63	V
Voltage of LPDDR4x	LPDDR4x VDD1	-0.4	2.3	V
	LPDDR4x VDD2	-0.4	1.6	V
	LPDDR4x VDDQ	-0.4	1.6	V
Storage temperature		-40	80	℃

Recommended Operating Conditions

You are recommended to operate the module in the following conditions to achieve optimized performance of the module.

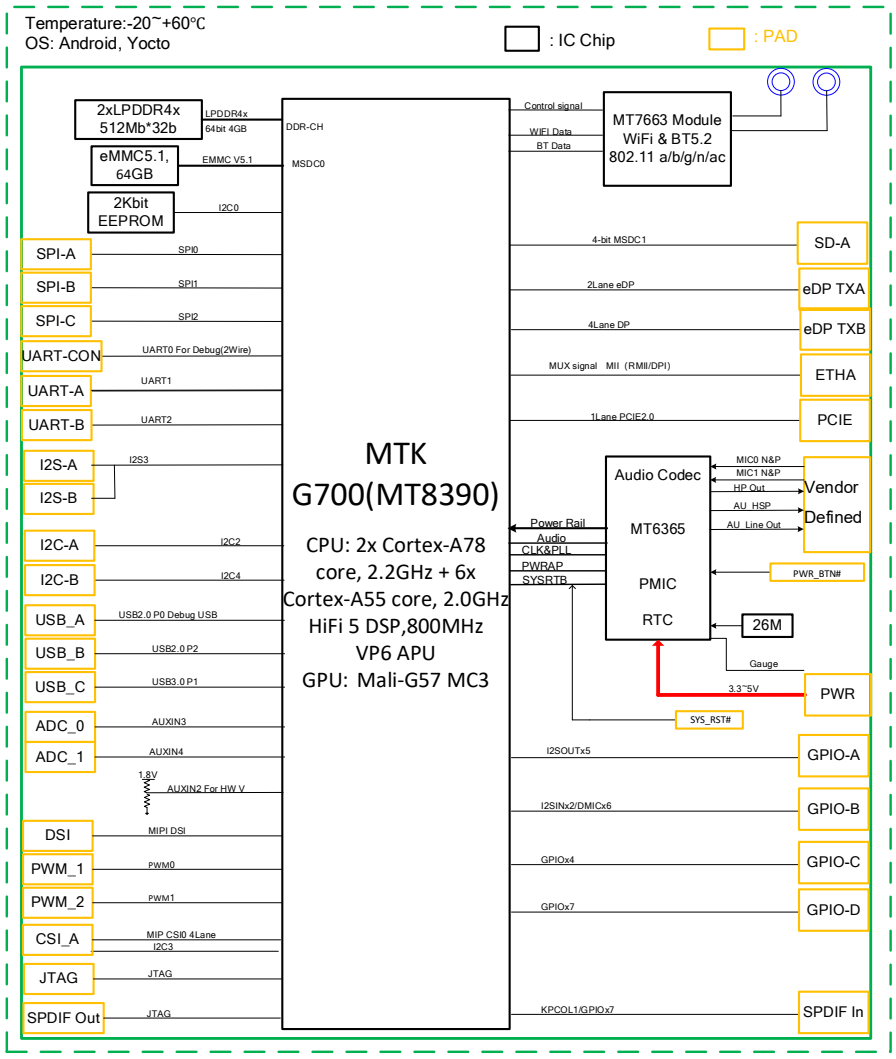
Parameter		Min.	Typ.	Max.	Unit
Voltage of the SOM		2.6	3.7	5	V
Voltage of EMCP	eMMC VCC	2.7	3.3	3.6	V
	eMMC VCCQ	1.7	1.8	1.95	V
	LPDDR4x VDD1	1.7	1.8	1.95	V
	LPDDR4x VDD2	1.06	1.1	1.17	V
	LPDDR4x VDDQ	1.06	1.1	1.17	V

(To be continued…)

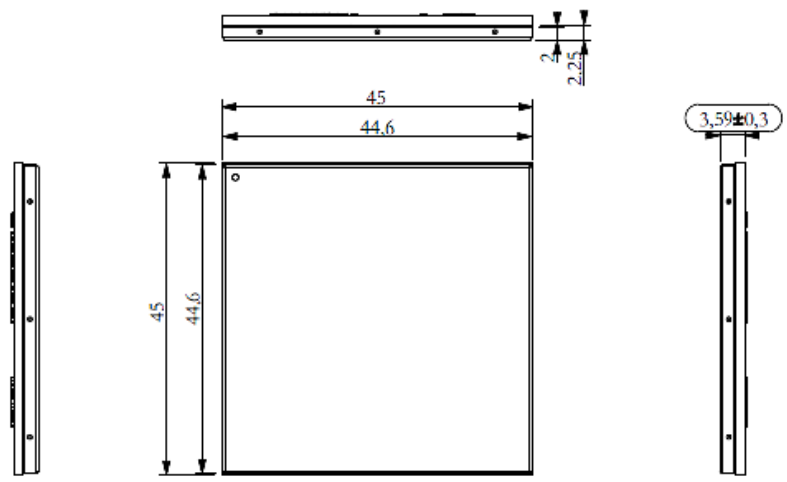
Recommended Operating Conditions (Cont'd)

Parameter		Min.	Typ.	Max.	Unit
Voltage on Wi-Fi/BT chip	AVDD18	1.6	1.8	1.9	V
	AVDD33	NA	3.3	3.63	V
Voltage on CPU	DVDD_CORE	0.52	0.75	0.81	V
	DVDD_SRAM_CORE	0.57	0.75	0.81	V
	DVDD_ADSP	0.71	0.75	0.81	V
	DVDD_SRAM_MM	0.57	0.75	0.81	V
	DVDD_MM	0.52	0.75	0.81	V
	DVDD_GPU	0.55	0.75	0.86	V
	DVDD_SRAM_GPU	0.57	0.85	0.92	V
	DVDD_PROC_B	0.52	0.85	1.19	V
	DVDD_SRAM_PROC_B	0.57	0.85	1.19	V
	DVDD_PROC_L	0.52	0.75	0.97	V
	DVDD_SRAM_PROC_L	0.57	0.85	1.08	V
	DVDD_APU	0.53	0.85	0.84	V
	DVDD_SRAM_APU	0.57	0.75	0.86	V
	AVDD075_EMI	0.675	0.75	0.825	V
	AVDD12_EMI	1.08	1.2	1.32	V
	AVDD18_EMI	1.62	1.8	1.98	V
	AVDD2_EMI	1.06	1.1	1.17	V
	AVDDQ_EMI	0.57	0.6	0.65	V

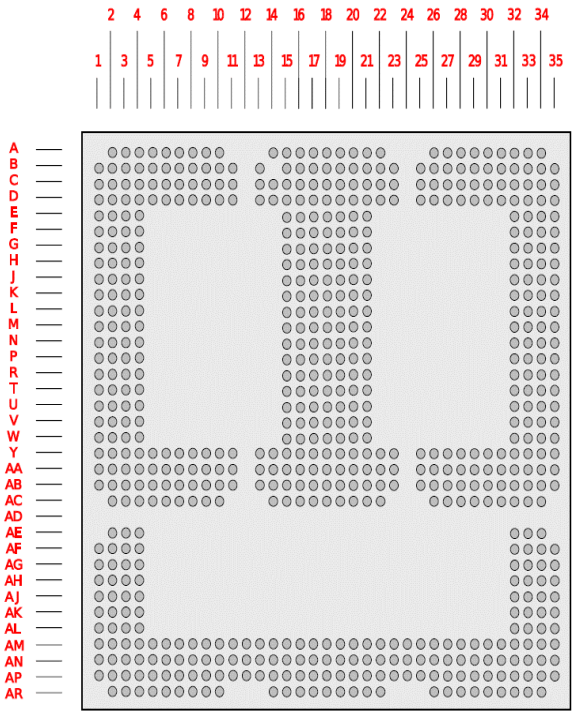
Block Diagram



Product Outlines



Pinout



(View from top, through the module)

Pin	Signal*	CPU Pad Name*	Description
U19, R18, W17, M19	NC		No connection
V17	EXT_EN	DSI1_LCM_RST	GPIO
T17	KPCOL0	KPCOL0	To enter recovery mode if carrier board is at low level
AA9	PWRKEY	PWRKEY (PMIC)	Power button input from carrier board. Carrier to float the line in inactive state. Active low, level sensitive. Should be de-bounced on the module
U17	SYSRSTB	SYSRSTB	System reset input from carrier board, active low
AB18	VCC_BAT		Power input, battery voltage
AA18	VCC_BAT		Power input, battery voltage
Y16, Y20, Y3, C5, AA33, B29	NC		No connection
Y17, Y8, Y9	NC		No connection
Y10, Y11, AE4, AF4, AG4	NC		No connection
Y25, Y26, Y27, Y28	VCC_IN_5V		5V power input
AH3, AH4, AJ3, AJ4, AK4, Y19, U18	NC		No connection
D18, E15, E21, F16, F20, J16	GND		Ground
J20, L18, M16, M20, P18	GND		Ground
R16, R20, V16, V20, Y18	GND		Ground

* Signal refers to the pin name used by Vantron.

* CPU Pad Name refers to corresponding pad name on the G700 CPU.

Pin	Signal	CPU Pad Name	Description
AA14, AA17, AA19, AA22, AB15, AB21	GND		Ground
A4, A7, A10, B2, B5, B8, B9, C11, D1, D5	GND		Ground
D8, E2, H2, H4, L2, L4, P2, P4, R1, U2	GND		Ground
U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AB3	GND		Ground
AA10, AA11, AB6, AB9, AC4, AC7, AC10	GND		Ground
A26, A29, A32, B27, B28, B30, B33, C25	GND		Ground
C32, C35, D28, D34, F33, F35, G34, H32	GND		Ground
J33, J35, K34, M35, N34, T34, W34, AE2	GND		Ground
AA25, AA26, AA27, AA28, AA32, AB28	GND		Ground
AB31, AB34, AC27, AC30, AC33, AE34	GND		Ground
AG3, AH2, AK3, AL2, AF35, AH34, AJ35	GND		Ground
AL34, AM13, AM16, AM19, AM22, AM35	GND		Ground
AN3, AN6, AN9, AP2, AN11, AN15, AN18	GND		Ground
AN21, AN33, AP5, AP8, AP13, AP16	GND		Ground
AP19, AP22, AP25, AP28, AP31, AP34	GND		Ground
AR14, AR17, AR20, AR26, AR29, AR32	GND		Ground
T18, T19, Y13, Y14, AA13, N2, AA2, J32	NC		No connection
K32, K33, L32, M32, M33, N32, P32, P34	NC		No connection
R32, R33, T32, T33, AB25, AB26, AE32	NC		No connection
AL3, AL4, AM3, AM4, AM5, AM6	NC		No connection
AM7, AM8, AM9, AM10, AM23, AM24	NC		No connection
AM25, AM26, AM27, AM28, AM29	NC		No connection
AM30, AM31, AN2, AN5, AN7, AN8	NC		No connection
AN24, AN25, AN26, AN27, AN28, AN29	NC		No connection

(To be continued…)

Pin	Signal	CPU Pad Name	Description
AN30, AN31, AP10	NC		No connection
C2	CMMCLK0	CMMCLK0	Camera reference clock/GPIO
G3	MAINCAM_PDN	CMMPDN0	Camera power down signal output, high active/GPIO
G4	MAINCAM_RST	CMMRST0	Camera interrupt signal input/GPIO
B3	CSI0A_L2N	CSI0A_L2N_T1C	Channel input CSI0A clock N
B4	CSI0A_L2P	CSI0A_L2P_T1B	Channel input CSI0A clock P
C1	CSI0A_L1N	CSI0A_L1N_T1A	Channel input CSI0A lane 0 N
B1	CSI0A_L1P	CSI0A_L1P_T0C	Channel input CSI0A lane 0 P
A2	CSI0B_L0N	CSI0B_L0N_T0B	Channel input CSI0B lane 1 N
A3	CSI0B_L0P	CSI0B_L0P_T0A	Channel input CSI0B lane 1 P
A5	CSI0A_L0N	CSI0A_L0N_T0B	Channel input CSI0A lane 2 N
A6	CSI0A_L0P	CSI0A_L0P_T0A	Channel input CSI0A lane 2 P
B6	CSI0B_L1N	CSI0B_L1N_T1A	Channel input CSI0B lane 3 N
B7	CSI0B_L1P	CSI0B_L1P_T0C	Channel input CSI0B lane 3 P
C4	SCL3	SCL5	I2C3 clock / GPIO
C3	SDA3	SDA5	I2C3 data / GPIO
F4	LCD_IO_EN_1V8	DSI1_DSI_TE	GPIO
E18	DISP_PWM	DSIP_PWM0	Backlight PWM signal for primary display / GPIO
F3	LCD_IO_EN_3V3	DSI0_LCM_RST	GPIO
AB8	DSI_CKN	DSI0_CKN_T1C	MIPI_DSI differential clock lane -
AB7	DSI_CKP	DSI0_CKP_T1B	MIPI_DSI differential clock lane +
AB11	DSI_D0N	DSI0_D0N_T1A	MIPI_DSI differential lane 0 -
AB10	DSI_D0P	DSI0_D0P_T0C	MIPI_DSI differential lane 0 +
AC9	DSI_D1N	DSI0_D1N_T2B	MIPI_DSI differential lane 1 -
AC8	DSI_D1P	DSI0_D1P_T2A	MIPI_DSI differential lane 1 +
AC6	DSI_D2N	DSI0_D2N_T0B	MIPI_DSI differential lane 2 -
AC5	DSI_D2P	DSI0_D2P_T0A	MIPI_DSI differential lane 2 +
AB5	DSI_D3N	DSI0_D3N	MIPI_DSI differential lane 3 -
AB4	DSI_D3P	DSI0_D3P_T2C	MIPI_DSI differential lane 3 +
AA3	EXT_WOL	DSI0_DSI_TE	GPIO
M18	AUXIN3	AUXIN3	Analog-digital converter 0
N18	AUXIN4	AUXIN4	Analog-digital converter 1

Pin	Signal	CPU Pad Name	Description
AC18, P19, C18, P16	NC		No connection
R19	JTRST	JTRST	JTAG reset, active low, suggest not using
N17	JTCK	JTCK	JTAG clock, suggest not using
P17	JTDI	JTDI	JTAG data input, suggest not using
R17	JTDO	JTDO	JTAG data output, suggest not using
N19	JTMS	JTMS	JTAG mode select, suggest not using
B22	SPDIF_IN	GPIO05	SPDIF data input
C16	SPDIF_OUT	GPIO11	SPDIF data output
D6	ACCDET	ACCDET (PMIC)	Accessory detection
D7	HP_EINT	HP_EINT (PMIC)	Headphone detection
Y29	AU_VIN0_N	AU_VIN0_N (PMIC)	Microphone channel 0 negative input
Y30	AU_VIN1_N	AU_VIN1_N (PMIC)	Microphone channel 1 negative input
Y31	AU_LOLN	AU_LOLN (PMIC)	Line out negative output
AA29	AU_VIN0_P	AU_VIN0_P (PMIC)	Microphone channel 0 positive input
AA30	AU_VIN1_P	AU_VIN1_P (PMIC)	Microphone channel 1 positive input
AA31	AU_LOLP	AU_LOLP (PMIC)	Line out positive output
AK32	FCHR_ENB	HOMEKEY (PMIC)	Force charging enable
AK33	AU_HPL	AU_HPL (PMIC)	Left channel output of the headphone
AL32	AU_HPR	AU_HPR (PMIC)	Right channel output of the headphone
AL33	AU_REFN	AU_REFN (PMIC)	Audio reference ground
AM32	CS_N	CS_N (PMIC)	Fuel gauge ADC input negative
AM33	CS_P	CS_P (PMIC)	Fuel gauge ADC input positive
F18	PWM_0	DISP_PWM1	Pulse width modulation port 0
A14	URXD1	UART1_RXD	UART1 receive data
B13	UTXD1	UART1_TXD	UART1 transmit data
G18, H18, J18, K18	NC		No connection
AB17, AC17, AB19, AC19	NC		No connection
C14, C13, D16, D15	NC		No connection
D14	URXD2	UART2_RXD	UART2 receive data
D13	UTXD2	UART2_TXD	UART2 transmit data

(To be continued…)

Pin	Signal	CPU Pad Name	Description
A22	NC		No connection
B23	NC		No connection
D22	URXD0	UART0_RXD	UART0 receive data, for debugging (1.8V)/GPIO
D23	UTXD0	UART0_TXD	UART0 transmit data, for debugging (1.8V)/GPIO
C22, C23, V21	NC		No connection
W21	I2SO2_D0	I2SO2_D0	I2S digital audio output 0
V19, W19	NC		No connection
W20	I2SIN_BCK	I2SO2_BCK	I2S digital audio clock
W18	I2SIN_LRCK	I2SO2_WS	I2S left-right channel synchronization clock
V18	I2SIN_MCK	I2SO2_MCK	I2S master clock output to I2S codec
AB2	PCIEG2_LN0_RXN	PCIE_LN0_RXN	PCIE 2.0 Lane 0 receive data -
AB1	PCIEG2_LN0_RXP	PCIE_LN0_RXP	PCIE 2.0 Lane 0 receive data +
AC3	PCIEG2_LN0_TXN	PCIE_LN0_TXN	PCIE 2.0 Lane 0 transmit data -
AC2	PCIEG2_LN0_TXP	PCIE_LN0_RXN	PCIE 2.0 Lane 0 transmit data +
V2	PCIE_PERESET_N	PCIE_PERESET_N	PCIE 2.0 preset signal output
M34, L34, L35, K35, L33	NC		No connection
W2	PCIE_CLKREQ0	PCIE_LCKREQ_N	PCIE 2.0 request reference clock
Y1	PCIEG2_CLK_N	PCIE_CKN	PCIE 2.0 Lane 0 reference clock output -
W1	PCIEG2_CLK_P	PCIE_CKP	PCIE 2.0 Lane 0 reference clock output +
R2, T1, U1	NC		No connection
T2	PCIE_PEWAKE#	PCIE_WAKE_N	PCIE2.0 wake signal
D11	USB_DP_P0	USB_DP_P0	USB differential data pairs for port C
D10	USB_DM_P0	USB_DM_P0	USB differential data pairs for port C
C10	USB0_DRV_VBUS	USB0_DRV_VBUS	USB power enable signal output for port C
D9	USB0_IDDIG	USB0_IDDIG	USB OTG device detection
C8	USB_OC_P1	I2SO2_D2	USB over-current signal input for port C
B11, B10	NC		No connection
A9, A8	NC		No connection
C9	USB_VBUS		USB port C power detection
D26	USB_DM_P1	USB_DP_P1	USB differential data pairs for port D
D25	USB_DP_P1	USB_DM_P1	USB differential data pairs for port D

Pin	Signal	CPU Pad Name	Description
C26	HOST3_EN	USB1_DRV_VBUS	USB power enable signal output for port D
D27	NC		No connection
C28	HOST3_OC	I2SO2_D3	GPIO
B26	SSUSB_RXN	SSUSB_RXN	Differential receive signal for SuperSpeed port D
B25	SSUSB_RXP	SSUSB_RXP	Differential receive signal for SuperSpeed port D
A28	SSUSB_TXN	SSUSB_TXN	Differential transmit signal for SuperSpeed port D
A27	SSUSB_TXP	SSUSB_TXP	Differential transmit signal for SuperSpeed port D
C27	NC		No connection
AA15	I2C_SCL0	SCL0	I2C port A clock
AA16	I2C_SDA0	SDA0	I2C port A data
AA20	I2C_SCL2	SCL2	I2C port B clock
AA21	I2C_SDA2	SDA2	I2C port B data
AB13	USB_DM_P2	USB_DM_P2	USB differential data pairs for port A
AC14	USB_DP_P2	USB_DP_P2	USB differential data pairs for port A
AC16	HOST2_EN	USB2_DRV_VBUS	USB power enable signal output for port A
AB14, AB16	NC		No connection
AC15	HOST2_OC	USB2_IDDIG	USB over-current signal input for port A
AB20	USB_VBUS_P2		USB port B power detection
AB23, AC22	NC		No connection
AC20, AB22	NC		No connection
AC21, AB20	NC		No connection
J21	SDMMC0_DET	DPI_D14	SDIO card detection
F21	MSDC1_CLK	MSDC1_CLK	SDIO clock
E20	MSDC1_CMD	MSDC1_CMD	SDIO command/response
G20	MSDC1_DAT0	MSDC1_DAT0	SDIO data line 0
G21	MSDC1_DAT1	MSDC1_DAT1	SDIO data line 1
H20	MSDC1_DAT2	MSDC1_DAT2	SDIO data line 2
H21	MSDC1_DAT3	MSDC1_DAT3	SDIO data line 3
C20, T21, K20	NC		No connection
D21	SDMMC0_PWR_EN	DPI_VSYNC	SDIO power enable
D20	SDMMC0_WP	SCL6	SDIO write protection
K21, L20, L21	NC		No connection
M21, N20, N21	NC		No connection
P20, P21, R21	NC		No connection

(To be continued…)

Pin	Signal	CPU Pad Name	Description
T20	VIO18_PMU		SDIO voltage
U21, U20	NC		No connection
D17	GPIO_A_0	GPIO02	GPIO_A_0
E17	GPIO_A_1	GPIO06	GPIO_A_1
F17	GPIO_A_2	GPIO07	GPIO_A_2
G17	GPIO_A_3	GPIO12	GPIO_A_3
H17	GPIO_A_4	GPIO13	GPIO_A_4
J17	GPIO_A_5	GPIO14	GPIO_A_5
D19	GPIO_B_0	GPIO15	GPIO_B_0
E19	GPIO_B_1	GPIO17	GPIO_B_1
F19	GPIO_B_2	I2SIN_D1	GPIO_B_2
G19	GPIO_B_3	I2SIN_D3	GPIO_B_3
H19	GPIO_B_4	USB2_VBUS_VALID	GPIO_B_4
J19	GPIO_B_5	DPI_HSYNC	GPIO_B_5
K19	GPIO_B_6	CMMCLK1	GPIO_B_6
L19	GPIO_B_7	CMMPDN1	GPIO_B_7
D3	GPIO_C_0	I2SIN_MCK	GPIO_C_0
D4	GPIO_C_1	CMMRST1	GPIO_C_1
E3	GPIO_C_2	I2SIN_BCK	GPIO_C_2
E4	NC		No connection
U32	GPIO_D_0	GPIO08	GPIO_D_0
U33	GPIO_D_1	GPIO09	GPIO_D_1
V32	GPIO_D_2	I2SIN_D2	GPIO_D_2
V33	GPIO_D_3	GPIO10	GPIO_D_3
W32	GPIO_D_4	DMIC1_CLK	GPIO_D_4
W33	GPIO_D_5	DMIC1_DAT	GPIO_D_5
Y32	GPIO_D_6	DMIC2_DAT	GPIO_D_6
AF32	GPIO_E_0	I2SIN_D0	GPIO_E_0
AF33	GPIO_E_1	I2SO2_D1	GPIO_E_1
AG32	GPIO_E_2	DMIC1_DAT_R	GPIO_E_2
AG33	GPIO_E_3	DMCI2_DAT_R	GPIO_E_3
AH32	GPIO_E_4	DPI_DE	GPIO_E_4
AH33	GPIO_E_5	DPI_CK	GPIO_E_5
AJ32, AJ33	NC		No connection
W15	SPIM0_MIO3	SPIM0_MIO3	SPI A serial interrupt
W16	SPIM0_MIO2	SPIM0_MIO2	SPI A write protection
Y15	SPIM0_CSB	SPIM0_CSB	SPI A master chip selection 0/ IO*CONN_TEST_CK
K17	NC		No connection
U16	SPIM0_CLK	SPIM0_CLK	SPI A serial clock

Pin	Signal	CPU Pad Name	Description
U15	SPIM0_MISO	SPIM0_MISO	SPI A master in slave out
V15	SPIM0_MOSI	SPIM0_MOSI	SPI A master out slave in
AA23	SPIM1_CSB	SPIM1_CSB	SPI B master chip selection 0
L17	NC		No connection
Y21	SPIM1_CLK	SPIM1_CLK	SPI B serial clock
Y22	SPIM1_MISO	SPIM1_MISO	SPI B master in slave out
Y23	SPIM1_MOSI	SPIM1_MOSI	SPI B master out slave in
C30	SPIM2_CSB	SPIM2_CSB	SPI C master chip selection 0
Y33	DMIC2_CLK	DMIC2_CLK	Not used
D29	SPIM2_CLK	SPIM2_CLK	SPI C serial clock
C29	SPIM2_MISO	SPIM2_MISO	SPI C master in slave out
D30	SPIM2_MOSI	SPIM2_MOSI	SPI C master out slave in
F15	NC		No connection
E16	ENET_RGMII_RXCTL	DPI_D10	Port A receive control
R15	ENET_RGMII_RXCLK	DPI_D9	Port A receive clock
M15	ENET_RGMII_RXCTL	DPI_D10	Port A receive data validation
L16	ENET_RGMII_RXER	DPI_D15	Port A receive error signal
N15	ENET_RGMII_RXD2	DPI_D5	Port A receive data bit 2
P15	ENET_RGMII_RXD3	DPI_D4	Port A receive data bit 3
J15	ENET_RGMII_TXCLK	DPI_D8	Port A transmit clock
K16	ENET_RGMII_TXCTL	DPI_D11	Port A transmit enable (Error)
K15	ENET_RGMII_RXD0	DPI_D7	Port A receive data bit 0 (receive first)
L15	ENET_RGMII_RXD1	DPI_D6	Port A receive data bit 1
H15	ENET_RGMII_TXD0	DPI_D3	Port A transmit data bit 0 (transmit first)
G15	ENET_RGMII_TXD1	DPI_D2	Port A transmit data bit 1
H16	ENET_RGMII_TXD2	DPI_D1	Port A transmit data bit 2
G16	ENET_RGMII_TXD3	DPI_D0	Port A transmit data bit 3
N16, E1, D2, P1, L1, K2, M1	NC		No connection
N1, H1, J2, J1, K1, G1, F1, G2	NC		No connection
F2, C6, C7, M2, AB35, AC34	NC		No connection
W35, T35, U34, R35, P35, N35	NC		No connection
M17	VIO18_PMU		1.8V IO power for all Ethernet interfaces
T16	EXT_MDC	DPI_D12	ETH management bus clock
T15	EXT_MDIO	DPI_D13	ETH management bus data
AR18	WIFI0_ANT		Wi-Fi antenna

(To be continued…)

Pin	Signal	CPU Pad Name	Description
AR21	BT_ANT		Bluetooth antenna
AR19, AR22, AP20, AP21	GND		Ground
A15, A17, A18	GND		Ground
A21, B15, B16	GND		Ground
B17, B18, B19	GND		Ground
B20, B21	GND		Ground
C34	EDPAUXN	EDPAUXN	eDP aux. signal output
C33	EDPAUXP	EDPAUXP	eDP aux. signal output
D31	DISP_BL_EN1	I2SIN_WS	LCD backlight enable
C31	DISP_PWM1	CMMCLK2	LCD backlight PWM
A31	EDP_LN0_TXN	EDP_LN0_TXN	eDP Lane 0 data output
A30	EDP_LN0_TXP	EDP_LN0_TXP	eDP Lane 0 data output
B32	EDP_LN1_TXN	EDP_LN1_TXN	eDP Lane 1 data output
B31	EDP_LN1_TXP	EDP_LN1_TXP	eDP Lane 1 data output
H33	DPAUXN	DPAUXN	DP aux. signal output
G33	DPAUXP	DPAUXP	DP aux. signal output
G32	DP_HPD	DPTX_HPD	DP hot plug signal input
E35	DP_LN0_TXN	DP_LN0_TXN	DP Lane 0 data output
D35	DP_LN0_TXP	DP_LN0_TXP	DP Lane 0 data output
F34	DP_LN1_TXN	DP_LN1_TXN	DP Lane 1 data output
E34	DP_LN1_TXP	DP_LN1_TXP	DP Lane 1 data output
H35	DP_LN2_TXN	DP_LN2_TXN	DP Lane 2 data output
G35	DP_LN2_TXP	DP_LN2_TXP	DP Lane 2 data output
J34	DP_LN3_TXN	DP_LN3_TXN	DP Lane 3 data output
H34	DP_LN3_TXP	DP_LN3_TXP	DP Lane 3 data output
AP17, AP18, AR15, AP15	GND		Ground
AR16	WIFI1_ANT		Wi_Fi antenna
AN16	HDMITX21_CLK_M	HDMITX21_CLK_M	HDMITX TMDS clock
AN17	HDMITX21_CLK_P	HDMITX21_CLK_P	HDMITX TMDS clock
AM20	HDMITX21_CH0_M	HDMITX21_CH0_M	HDMITX TMDS data lane 0
AM21	HDMITX21_CH0_P	HDMITX21_CH0_P	HDMITX TMDS data lane 0
AN19	HDMITX21_CH1_M	HDMITX21_CH1_M	HDMITX TMDS data lane 1
AN20	HDMITX21_CH1_P	HDMITX21_CH1_P	HDMITX TMDS data lane 1
AM17	HDMITX21_CH2_M	HDMITX21_CH2_M	HDMITX TMDS data lane 2
AM18	HDMITX21_CH2_P	HDMITX21_CH2_P	HDMITX TMDS data lane 2
AM14	HDMITX_HTPLG	HDMITX_HTPLG	HDMI hot plug detection
AM15	HDMITX_CEC	HDMITX_CEC	HDMI CEC
AM11	HDMITX_SCL	HDMITX_SCL	HDMI serial clock
AM12	HDMITX_SDA	HDMITX_SDA	HDMI serial data

* Apart from those specified here, any pins not included in these sheets are not connected.

Ordering Information

Ordering No.	Operating system	Packaging	Memory	Storage
VOSM700-A	Android	LGA	4GB LPDDR4	64GB eMMC
VOSM700-Y	Yocto	LGA	4GB LPDDR4	64GB eMMC

Packing list	
VOSM700 system-on-module	1

Company Profile

Since its establishment in 2002 by two Silicon Valley entrepreneurs, Vantron Technology has been at the forefront of the connected IoT devices and IoT platform solutions. Today, Vantron boasts a global customer base that includes many Fortune Global 500 companies. Its product lines cover edge intelligent hardware, IoT communication devices, industrial displays and BlueSphere cloud platforms.

With over 20 years of experience in R&D of intelligent edge hardware including SOMs, motherboards, and embedded industrial computers, Vantron has provided users with diverse embedded solutions featuring ARM and X86 architectures. Its offerings range from Linux, Android to Windows, from embedded level to desktop level, and from gateways to servers. In addition, it provides services such system trimming, driver transplantation and more to cater to the unique needs of its users.

