VOSM62P System-on-Module

Product Brief

The VOSM62P is a compact, feature-enhanced system-on-module (SOM) built around Texas Instruments' performance-optimized AM62P54 64-bit industrial Sitara SoC. Fully compliant with the Open Standard Module (OSM) form factor, it features an ultra-compact footprint, low power consumption, and comprehensive peripheral scalability, ideal for cost-sensitive industrial embedded edge deployments.

Powered by a quad-core Arm Cortex-A53 microprocessor subsystem at up to 1.4GHz plus a dedicated Cortex-R5F real-time MCU core, the module integrates 4GB LPDDR4 memory and 64GB industrial-grade eMMC flash storage, delivering reliable and efficient local data caching and program execution for continuous edge operation. It exposes a full set of industrial-grade peripherals via standard OSM pads, including dual Gigabit Ethernet, CAN FD, UART, GPIO, SPI, I^2C, and USB 2.0, enabling flexible device connection and field data acquisition. The module supports up to three independent displays via the MIPI DSI and LVDS interfaces, meeting mainstream industrial HMI and visual interaction demands.

Featuring TI's on-chip hardware security module, the VOSM62P provides robust end-to-end data security for payment terminals, portable medical devices, and other scenarios with high security requirements.

With Linux Yocto support and long-term software maintenance, the module greatly simplifies development and shortens customer time-to-market. It is an optimal solution for smart charging stations, building automation controllers, portable medical monitoring terminals, and industrial HMI equipment.

Features and benefits

VOSM62P
Quad-core Cortex-A53 microprocessor subsystem
Low-power design for high energy efficiency
Up to three independent displays via MIPI and LVDS
Rich I/O: USB, UART, I^2C, CAN FD, GPIO, SPI
Dual GbE MAC on module, Wi-Fi on carrier board
Arm TrustZone security technology
Linux Yocto operating system support
OSM size-L compliant (45mm x 45mm)
Extended service life (7+ years)

Application Scenarios

Smart EV Charging

Industrial HMI

Building Automation

Automotive Display

Remote Inspection

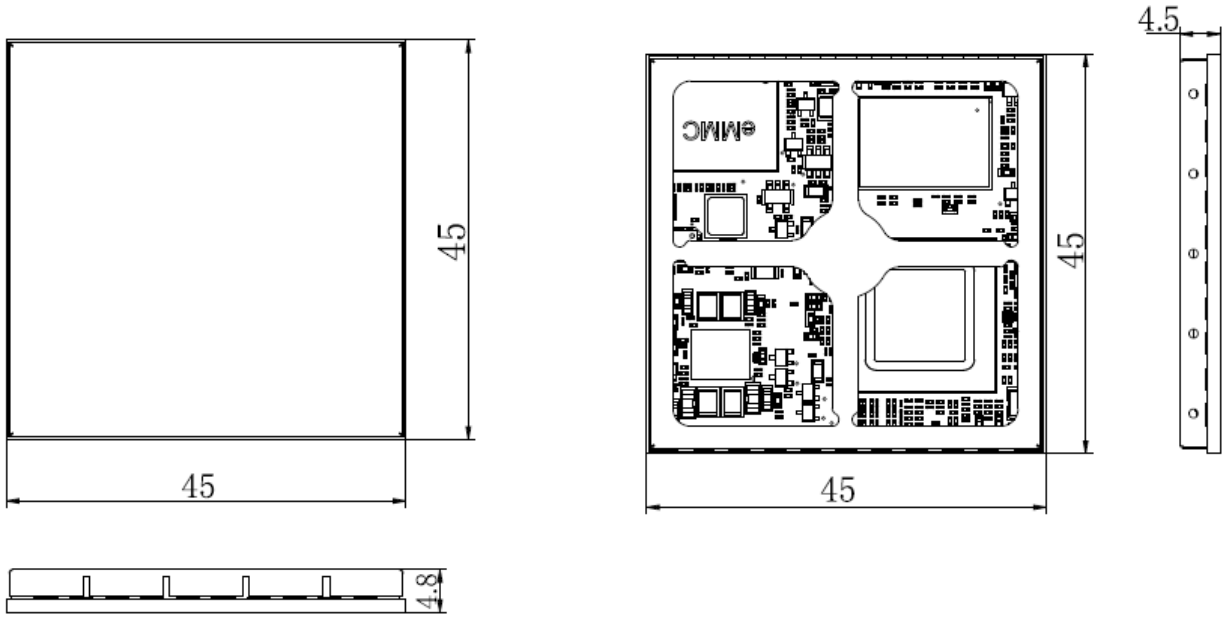
Portable Patient Monitor

VOSM62P System-on-Module Datasheet

Specifications			
System	CPU	TI AM62P54, Quad-core 64-bit Arm® Cortex®-A53 microprocessor, up to 1.4GHz	
	MCU	Single-core Arm® Cortex®-R5F, up to 800MHz for real-time processing	
		Single-core Arm® Cortex®-R5F, up to 800MHz for device management	
	GPU	Imagination IMG BXS-4-64, up to 50GFLOPS, API support: OpenGL ES 3.2, Vulkan 1.2	
	Memory	4GB LPDDR4	
	Storage	64GB eMMC 5.1	
Communication	Ethernet	GbE MAC (TSN)	
Media	Video processing	Hardware H.264/H.265 video encoder/decoder, up to 4K UHD (3840 × 2160)	
Power	Input	5V DC input	
Software	Operating system	Linux Yocto	
Mechanical	Dimensions	45mm x 45mm (OSM Size-L)	Packaging: LGA
Miscellaneous	RTC	Integrated RTC	
Environmental Condition	Temperature	Operating: -40℃ ~ +85℃	Storage: -40℃ ~ +85℃
	Humidity	5%~95% RH (Non-condensing)	

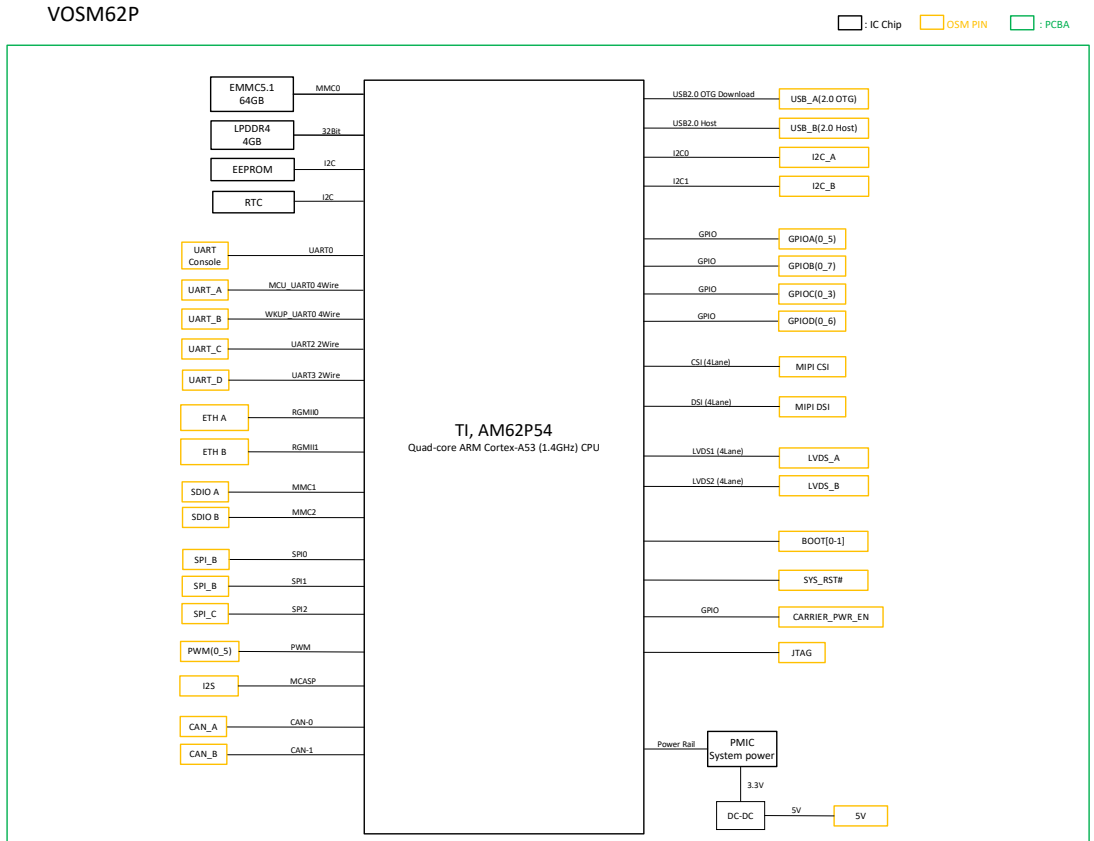
I/O	
Display (Triple-display output support:	1 × 4-Lane MIPI DSI D-PHY, up to 3840 × 1080 @60fps
MIPI + 2 × Independent LVDS)	2 × 4-Lane LVDS, up to 3840 × 1080 @60fps (Dual-Link) / 1920 × 1080 each (Independent)
Camera	1 × 4-Lane MIPI CSI-2 D-PHY, up to 2.5Gbps per lane (ECC/CRC error correction)
Audio	1 × I^2S, for carrier board codec
Ethernet	2 × RGMII, 10/100/1000Mbps, TSN supported
USB	1 × USB 2.0 OTG 1 × USB 2.0 Host
SDIO	2 × 4-bit SDIO
SPI	3 × SPI
I^2C	2 × I^2C
CAN	2 × CAN (CAN-FD supported)
UART	4 × Communication UART 1 × Debug UART
GPIO	25 × GPIO (Max.)
JTAG	Supported
PWM	5 × PWM for general use
Key Signal	1 × Reset key

Mechanical Outline



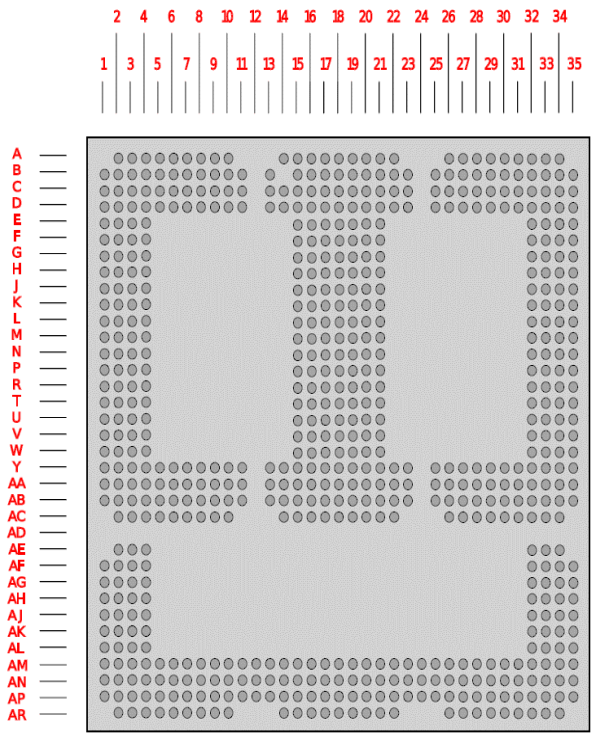
Block Diagram

VOSM62P



Temperature:
Operating: -40°C ~ +85°C
Storage: -40°C ~ +85°C

Pinout



(View from top, through the module)

In the tables below:

* **Pin** refers to the pin number defined by OSM as shown in above figure.

* **Signal** refers to the pin name used by Vantron.

* **CPU Ball #** refers to the corresponding designations of the AM62P54 CPU.

* Certain signals are derived from auxiliary ICs and the corresponding IC names are provided accordingly.

* Unless otherwise explicitly stated, all I/O signals use a **1.8V level**.

Pin*	Signal*	CPU Ball #*	Description
U19	BOOT_SEL0#	V25	BOOT config[0] BOOT config[1:0]=10=USB DFU BOOT config[1:0]=01=eMMC BOOT config[1:0]=00=SD Card
R18	BOOT_SEL1#	T20	BOOT config[1] BOOT config[1:0]=10=USB DFU BOOT config[1:0]=01=eMMC BOOT config[1:0]=00=SD Card
V17	CARRIER_PWR_EN	Y21	Carrier power control 1=ON; 0=OFF
T17	NC		No connection
AA9	NC		No connection
W17	RTC_VBAT		RTC power input (3V voltage)
U17	SYS_RST#	G22	RESET KEY 0=active; 1=inactive (PU 10K)
AB18, AA18, M19, Y16, Y20, Y3	NC		No connection
C5, AA33, Y17, Y8, Y9, Y10, Y11	NC		No connection
Y25, Y26, Y27, Y28	VCC_IN_5V		**5V** power input for the module
AE4, AF4, AG4, AH3	NC		No connection

Pin	Signal	CPU Ball #	Description
AH4, AJ3, AJ4, AK4 B29, Y19, U18	NC		No connection
D18, E15, E21, F16, F20, J16, J20, L18	GND		Ground
M16, M20, P18, R16, R20, V16, V20, Y18	GND		Ground
AA14, AA17, AA19, AA22, AB15, AB21, A4	GND		Ground
A7, A10, B2, B5, B8, B9, C11, D1, D5, D8	GND		Ground
E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3	GND		Ground
Y2, AA1 AA4, AA7 AA8, AA10, AA11, AB3	GND		Ground
AB6, AB9, AC4, AC7, AC10, A26, A29, A32	GND		Ground
B27, B28, B30, B33, C25, C32, C35, D28	GND		Ground
D34, F33, F35, G34, H32, J33, J35, K34	GND		Ground
M35, N34, T34, W34, AA25, AA26, AE2	GND		Ground
AA27, AA28, AA32, AB28, AB31, AB34	GND		Ground
AC27 AC30, AC33, AE34, AF35, AG3	GND		Ground
AH2, AK3, AL2, AH34, AJ35, AL34, AM13	GND		Ground
AM16, AM19, AM22, AM35, AN3, AN6	GND		Ground
AN9, AN11, AP2, AN15, AN18, AP5	GND		Ground
AN21, AN33, AP8, AP13, AP16, AP19	GND		Ground
AP22, AP25, AP28, AP31, AP34, AR14	GND		Ground
AR17, AR20, AR26, AR29, AR32	GND		Ground
T18, T19, Y13, Y14, AA13, N2, AA2, J32	NC		No connection
K32, K33, L32, M32, M33, N32, P32, P34	NC		No connection
R32, R33, T32, T33, AB25, AB26, AE32, AL3	NC		No connection
AL4, AM3, AM4, AM5, AM6, AM7, AM8, AM9	NC		No connection
AM10, AM23, AM24, AM25, AM26, AM27	NC		No connection

(To be continued…)

Pin	Signal	CPU Ball #	Description
AM28, AM29, AM30, AM31	NC		No connection
AN2, AN5, AN7, AN8, AN24,	NC		No connection
AN25, AN26, AN27, AN28,	NC		No connection
AN29, AN30, AN31, AP10, C2	NC		No connection
G3	CAM_PWR/GPIO_C_6	F23	Camera power enable / GPIO
G4	CAM_RST#/GPIO_C_7	B23	Camera reset / GPIO
B3	CSI_CLOCK_N	AE12	MIPI CSI differential clock -
B4	CSI_CLOCK_P	AE11	MIPI CSI differential clock +
C1	CSI_DATA0_N	AB11	MIPI CSI differential data 0 -
B1	CSI_DATA0_P	AB10	MIPI CSI differential data 0 +
A2	CSI_DATA1_N	AC10	MIPI CSI differential data 1 -
A3	CSI_DATA1_P	AC9	MIPI CSI differential data 1 +
A5	CSI_DATA2_N	AA10	MIPI CSI differential data 2 -
A6	CSI_DATA2_P	AA9	MIPI CSI differential data 2 +
B6	CSI_DATA3_N	AD9	MIPI CSI differential data 3 -
B7	CSI_DATA3_P	AD8	MIPI CSI differential data 4 +
C4	I2C_CAM_SCL/CSI_TX_P	T22	Camera I^2C serial clock
C3	I2C_CAM_SDA/CSI_TX_N	U25	Camera I^2C serial data
F4	LCD_BL_EN /GPIO_C_5	F25	Backlight enable for MIPI DSI display
E18	DISP_BL_PWM/PWM_0	B24	PWM dimming for MIPI DSI display
F3	DISP_VDD_EN/GPIO_C_4	F24	VDD logic enable for MIPI DSI display
AB8	MIPI_DSI1_CKN	AA12	MIPI DSI differential clock -
AB7	MIPI_DSI1_CKP	AA13	MIPI DSI differential clock +
AB11	MIPI_DSI1_DN0	AD11	MIPI DSI differential data 0 -
AB10	MIPI_DSI1_DP0	AD12	MIPI DSI differential data 0 +
AC9	MIPI_DSI1_DN1	AB13	MIPI DSI differential data 1 -
AC8	MIPI_DSI1_DP1	AB14	MIPI DSI differential data 1 +
AC6	MIPI_DSI1_DN2	AC12	MIPI DSI differential data 2 -
AC5	MIPI_DSI1_DP2	AC13	MIPI DSI differential data 2 +
AB5	MIPI_DSI1_DN3	AE14	MIPI DSI differential data 3 -
AB4	MIPI_DSI1_DP3	AE15	MIPI DSI differential data 3 +
AA3, M18, N18	NC		No connection
AC18, P19, C18	NC		No connection
R19	JTAG_TRSTN	B13	JTAG test reset, active low
N17	JTAG_TCK (SWCLK)	C13	JTAG test clock
P17	JTAG_TDI	E13	JTAG test data in
R17	JTAG_TDO (SWO)	C14	JTAG test data out
N19	JTAG_TMS (SWDIO)	E14	JTAG test mode select

MIPI CSI × 4-lane (MIPI CSI voltage)

Pin	Signal	CPU Ball #	Description
C18, B22, C16	NC		No connection
F18	PWM_1	E24	Pulse width modulation 1
G18	PWM_2	G20	Pulse width modulation 2
H18	PWM_3	G23	Pulse width modulation 3
J18	PWM_4	E25	Pulse width modulation 4
K18	PWM_5	D25	Pulse width modulation 5
AB17	CAN_A_RX	D6	CAN0 transmit data
AC17	CAN_A_TX	E8	CAN0 receive data
AB19	CAN_B_RX	F8	CAN1 transmit data
AC19	CAN_B_TX	E7	CAN1 receive data
C14	UART_A_CTS	B8	UART A clear to send
C13	UART_A_RTS	B7	UART A request to send
A14	UART_A_RX	B6	UART A receive data
B13	UART_A_TX	C8	UART A transmit data
D16	UART_B_CTS	C7	UART B clear to send
D15	UART_B_RTS	C6	UART B request to send
D14	UART_B_RX	D8	UART B receive data
D13	UART_B_TX	D7	UART B transmit data
A22	UART_C_RX	AE24	UART C receive data
B23	UART_C_TX	W23	UART C transmit data
D22	UART_CON_RX	A22	Debug UART receive data
D23	UART_CON_TX	B22	Debug UART transmit data
C22	UART_D_RX	AA23	UART D receive data
C23	UART_D_TX	Y23	UART D transmit data
V21	I2S_A_DATA_IN	T25	I2S receive data
W21	I2S_A_DATA_OUT	R25	I2S transmit data
V19	NC		No connection
W19	NC		No connection
W20	NC		No connection
W18	I2S_LRCLK	AA24	I2S word select
V18	I2S_MCLK	U24	I2S master clock
AA15	I2C_A_SCL	B25	I2C A serial clock (PU 4.7k)
AA16	I2C_A_SDA	A24	I2C A serial data (PU 4.7k)
AA20	I2C_B_SCL	T22	I2C B serial clock (PU 4.7k)
AA21	I2C_B_SDA	U25	I2C B serial data (PU 4.7k)
AB13	USB_A_D_N	AE8	USB A high-speed data -
AC14	USB_A_D_P	AE7	USB A high-speed data +
AC16	USB_A_EN	W21	USB-A enable
AB16	USB_A_VBUS	Y10	USB-A VBUS (**5V**)
AB23	USB_B_D_N	AE10	USB B high-speed data -
AC22	USB_B_D_P	AE9	USB B high-speed data +
AC20	USB_B_EN	W20	USB-B enable
AB20	USB_B_VBUS	Y7	USB-B VBUS (**5V**)

(To be continued…)

Pin	Signal	CPU Ball #	Description
J21	NC		No connection
F21	SDIO_A_CLK	K21	SDIO A clock output
E20	SDIO_A_CMD	K24	SDIO A bidirectional command
G20	SDIO_A_D0	K23	SDIO A data 0
G21	SDIO_A_D1	H23	SDIO A data 1
H20	SDIO_A_D2	H22	SDIO A data 2
H21	SDIO_A_D3	H25	SDIO A data 3
C20	NC		No connection
D21	SDIO_A_PWR_EN	P22	SDIO A power enable
D20	NC		No connection
T21	NC		No connection
K20	SDIO_B_CLK	J24	SDIO B clock output
K21	SDIO_B_CMD	H20	SDIO B bidirectional command
L20	SDIO_B_D0	H21	SDIO B data 0
L21	SDIO_B_D1	H23	SDIO B data 1
M21	SDIO_B_D2	H22	SDIO B data 2
N20	SDIO_B_D3	H25	SDIO B data 3
N21, P20, P21, R21, T20	NC		No connection
U21	SDIO_B_PWR_EN	T23	SDIO B power enable
U20	NC		No connection
D17	GPIO_A_0	N23	GPIO/defined on carrier
E17	GPIO_A_1	N24	GPIO/defined on carrier
F17	GPIO_A_2	AC23	GPIO/defined on carrier
G17	GPIO_A_3	AC22	GPIO/defined on carrier
H17	GPIO_A_4	AD21	GPIO/defined on carrier
J17	GPIO_A_5	AC21	GPIO/defined on carrier
D19	GPIO_B_0	P25	GPIO/defined on carrier
E19	GPIO_B_1	AD24	GPIO/defined on carrier
F19	GPIO_B_2	P24	GPIO/defined on carrier
G19	GPIO_B_3	AE23	GPIO/defined on carrier
H19	GPIO_B_4	AE22	GPIO/defined on carrier
J19	GPIO_B_5	AD23	GPIO/defined on carrier
K19	GPIO_B_6	AE21	GPIO/defined on carrier
L19	GPIO_B_7	AC20	GPIO/defined on carrier
D3	GPIO_C_0	L23	GPIO/defined on carrier
D4	GPIO_C_1	L25	GPIO/defined on carrier
E3	GPIO_C_2	M25	GPIO/defined on carrier
E4	GPIO_C_3	L24	GPIO/defined on carrier

Pin	Signal	CPU Ball #	Description
U32	GPIO_D_0	W22	GPIO/defined on carrier
U33	GPIO_D_1	T24	GPIO/defined on carrier
V32	GPIO_D_2	N25	GPIO/defined on carrier
V33	GPIO_D_3	M24	GPIO/defined on carrier
W32	GPIO_D_4	AA20	GPIO/defined on carrier
W33	GPIO_D_5	Y20	GPIO/defined on carrier
Y32	GPIO_D_6	AB23	GPIO/defined on carrier
AF32, AF33, AG32, AG33	NC		No connection
AH32, AH33, AJ32. AJ33	NC		No connection
Y15	SPI0_CS0	D20	SPI A master chip select 0
K17	SPI_A_CS1#/GPIO_A_6	E20	SPI A master chip select 1
U16	SPI_A_SCK	B21	SPI_A serial clock
U15	SPI_A_SDI_(IO0)	B20	SP A serial data in
V15	SPI_A_SDO_(IO1)	C21	SPI A serial data out
AA23	SPI_B_CS0#	N21	SPI B master chip select 0
L17	SPI_B_CS1#/GPIO_A_7	L22	SPI B master chip select 1
Y21	SPI_B_SCK	N22	SPI B serial clock
Y22	SPI_B_SDI	P21	SPI B serial data in
Y23	SPI_B_SDO	N20	SPI B serial data out
C30	SPI_C_CS0#	B10	SPI C master chip select 0
Y33	SPI_C_CS1#/GPIO_D_7	E10	SPI C master chip select 1
D29	SPI_C_SCK	C10	SPI C serial clock
C29	SPI_C_SDI	B11	SPI C serial data in
D30	SPI_C_SDO	D10	SPI C serial data out
F15	NC		No connection
E16	NC		No connection
R15	ETH_A_(R)(G)MII_RX_CLK	D19	RGMII A receive clock
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	F19	RGMII A receive control
N15	ETH_A_(R)(G)MII_RXD2	E17	RGMII A receive data 2
P15	ETH_A_(R)(G)MII_RXD3	C19	RGMII A receive data 3
J15	ETH_A_(R)(G)MII_TX_CLK	D16	RGMII A transmit clock
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	A20	RGMII A transmit control
K15	ETH_A_(S)(R)(G)MII_RXD0	E19	RGMII A receive data 0
L15	ETH_A_(S)(R)(G)MII_RXD1	E16	RGMII A receive data 1
H15	ETH_A_(S)(R)(G)MII_TXD0	B19	RGMII A transmit data 0
G15	ETH_A_(S)(R)(G)MII_TXD1	A21	RGMII A transmit data 1
H16	ETH_A_(S)(R)(G)MII_TXD2	D17	RGMII A transmit data 2
G16	ETH_A_(S)(R)(G)MII_TXD3	A19	RGMII A transmit data 3
N16	NC		No connection
E1	NC		No connection
D2	NC		No connection

(To be continued…)

Pin	Signal	CPU Ball #	Description
P1	ETH_B_(R)(G)MII_RX_CLK	A16	RGMII B receive clock
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	A15	RGMII B receive control
M1	ETH_B_(R)(G)MII_RXD2	A14	RGMII B receive data 2
N1	ETH_B_(R)(G)MII_RXD3	B14	RGMII B receive data 3
H1	ETH_B_(R)(G)MII_TX_CLK	B17	RGMII B transmit clock
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	B18	RGMII B transmit control
J1	ETH_B_(S)(R)(G)MII_RXD0	B15	RGMII B receive data 0
K1	ETH_B_(S)(R)(G)MII_RXD1	B16	RGMII B receive data 1
G1	ETH_B_(S)(R)(G)MII_TXD0	A18	RGMII B transmit data 0
F1	ETH_B_(S)(R)(G)MII_TXD1	C17	RGMII B transmit data 1
G2	ETH_B_(S)(R)(G)MII_TXD2	A17	RGMII B transmit data 2
F2	ETH_B_(S)(R)(G)MII_TXD3	C16	RGMII B transmit data 3
C6	ETH_B_MDC	F17	MDIO clock
C7	ETH_B_MDIO	F16	MDIO data
T16	ETH_MDC	F17	MDIO clock
T15	ETH_MDIO	F16	MDIO data
AN12	LVDS_A_CLK_N	AE18	LVDS A differential clock -
AN13	LVDS_A_CLK_P	AE17	LVDS A differential clock +
AP17	LVDS_A_LANE0_N	AE20	LVDS A data lane 0 -
AP18	LVDS_A_LANE0_P	AD20	LVDS A data lane 0 +

Pin	Signal	CPU Ball #	Description
AR15	LVDS_A_LANE1_N	AC19	LVDS A data lane 1 -
AR16	LVDS_A_LANE1_P	AD19	LVDS A data lane 1 +
AP14	LVDS_A_LANE2_N	AA19	LVDS A data lane 2 -
AP15	LVDS_A_LANE2_P	AB19	LVDS A data lane 2 +
AP11	LVDS_A_LANE3_N	AD19	LVDS A data lane 3 -
AP12	LVDS_A_LANE3_P	AE19	LVDS A data lane 3 +
AN16	LVDS_B_CLK_N	AD15	LVDS B differential clock -
AN17	LVDS_B_CLK_P	AD14	LVDS B differential clock +
AM20	LVDS_B_LANE0_N	AD17	LVDS B data lane 0 -
AM21	LVDS_B_LANE0_P	AD16	LVDS B data lane 0 +
AN19	LVDS_B_LANE1_N	AB17	LVDS B data lane 1 -
AN20	LVDS_B_LANE1_P	AC17	LVDS B data lane 1 +
AM17	LVDS_B_LANE2_N	AC16	LVDS B data lane 2 -
AM18	LVDS_B_LANE2_P	AC15	LVDS B data lane 2 +
AM14	LVDS_B_LANE3_N	AB16	LVDS B data lane 3 -
AM15	LVDS_B_LANE3_P	AA16	LVDS B data lane 3 +
AN23	LVDS_BL_EN	F20	LVDS backlight enable
AN22	LVDS_BL_PWM	C24	LVDS backlight PWM control
AM11	LVDS_I2C_CLK	B25	I2C clock for touch panel
AM12	LVDS_I2C_DAT	A24	I2C data for touch panel
AN14	LVDS_VDD_EN	U23	LVDS VDD power enable

* Apart from those specified here, any pins not included in these sheets are not used.

Ordering Information

Ordering No.	Memory	Storage	Connectivity	Description
VOSM62P	4GB DDR4	64GB eMMC	GbE	MIPI DSI, LVDS, SPI, CAN, UART, USB, I^2C, I^2S, GPIO
VT-SBC35-VOSM62P	4GB DDR4	16GB eMMC	GbE, Wi-Fi, Bluetooth	VOSM62P + Carrier board, MIPI DSI, UART, CAN, Audio, USB, GPIO

Packing List	
VOSM62P system-on-module	1

Company Profile

Since its establishment in 2002 by two Silicon Valley entrepreneurs, Vantron Technology has been at the forefront of the connected IoT devices and IoT platform solutions. Today, Vantron boasts a global customer base that includes many Fortune Global 500 companies. Its product lines cover edge intelligent hardware, IoT communication devices, industrial displays and BlueSphere cloud platforms.

With over 20 years of experience in R&D of embedded edge intelligent hardware, Vantron has provided users with diverse embedded solutions featuring ARM and X86 architectures. Its offerings range from Linux to Windows, from embedded to desktop level, and from gateway to server. In addition, it provides users with system trimming, driver transplantation and more to cater to the unique needs of its users.